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Grid Converters for Stationary Battery Energy Storage Systems

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GRID CONVERTERS FOR STATIONARY BATTERY ENERGY STORAGE SYSTEMS

IONUT TRINTIS

DISSERTATION SUBMITTED TO THE
FACULTY OF ENGINEERING & SCIENCE AT
AALBORG UNIVERSITY
IN CANDIDACY FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY IN ELECTRICAL ENGINEERING

RECOMMENDED FOR ACCEPTANCE
BY THE DEPARTMENT OF ENERGY TECHNOLOGY
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Abstract

The integration of renewable energy sources in the power system, with high percentage, is a well known challenge nowadays. Power sources like wind and solar are highly volatile, with fluctuations on various time scales. One long term solution is to build a continentwide or worldwide supergrid. Another solution is to use distributed energy storage units, and create virtual power plants. Stationary energy storage is a complementary solution, which can postpone the network expansion and can be optimized for different kind of grid services. As an energy storage solution with timing for few seconds to hours, rated at MW and MWh, battery energy storage systems are suitable and efficient solutions.

Grid connection of the storage system can be done at different voltage levels, depending on the location and application scenario. For high power and energy ratings, increase in the battery and converter voltage ratings can enhance the overall system efficiency.

This work is divided in two parts, "Control of DC-AC Grid Converters" and "Medium Voltage Grid Converters for Energy Storage". The first part starts with a brief review of control strategies applied to grid connected DC-AC converters. A control implementation was realized for a 100 kW active rectifier to be used in a 6 kV battery energy storage test bench. In the second part, different solutions for power converters to interface energy storage units to medium voltage grid are given. A new modular multilevel converter concept is introduced, where the energy storage units are integrated in each converter cell.

The control of DC-AC grid converters has been a research subject for more than a century, and there is still place for improvements. A review of the main control principles is given in the first part. The stationary frame control was implemented for a low-voltage 100 kW bidirectional grid converter, to be used in a high voltage battery energy storage test bench. The control structure proved to be stable without damping. The converter was tested in the test bench and the experimental results are presented.

Multilevel converters are replacing the classical two-level converters more and more, on a large variety of applications. For medium voltage applications, multilevel converters are a necessity. The second part presents a review of hard-switched and soft-switched multilevel converter topologies for medium voltage. Four converter topologies were chosen as potential solutions for direct connection of battery energy storage systems to the grid. An evaluation is done, in terms of semiconductors requirements and losses, output voltage quality and common mode voltage.

The main advantage of batteries direct connection to the grid is the high efficiency potential. However, this solution is suitable only for battery technologies with low voltage variation. It is also necessary to build a battery system with high amount of serial

connected cells, and the knowledge in this field is still limited nowadays. Therefore, two-stage converters solutions were introduced to overcome these disadvantages. Modular multilevel converters can make use of battery voltage technologies where the maturity and reliability is well proven in industry.

Cascaded H-bridge topology with bidirectional boost converters is proposed to interface low voltage batteries to the medium voltage grid. A control structure based on single phase control is proposed. It balances the capacitor voltages and the state of charge of batteries from different cells. A semiconductor loss analysis is performed and it shows the loss distribution in the converter cell and the efficiency over a wide battery voltage variation.

A new modular multilevel converter structure with integrated energy storage is introduced. This converter structure is suitable to interface low and medium voltage energy storage units to medium and high voltage grids. It can also interconnect a DC and AC grid with bidirectional power flow, where both can be backed-up for the distributed energy storage units installed in each converter cell. The converter operation and control methods are presented, and the energy storage system construction concept and challenges are addressed.

Acknowledgements

I will firstly like to express my gratitude to my supervisor, Prof. Stig Munk-Nielsen, for all his time and patience invested in this project. The endless interesting discussions we had during the PhD period created ideas, ground and shape for this work. Many thanks to my co-supervisor Prof. Remus Teodorescu for all this technical support based on straight-forward approaches. Discussions along the project helped to clarify to myself many of the technical issues in grid connected converters and power systems that integrate power converters.

I would like to acknowledge the financial support from the E.ON AG, under the E.ON Research Initiative, the call on Energy Storage with the project 2007/B4-Highly Efficient and Reliable Modular Battery Energy Storage Systems (HERMES). I would also like to acknowledge the supervisors from E.ON UK for the good cooperation and good understanding they had during the project, and in particular to Matthew Knight and Stuart Norman. I acknowledge the financial support also from Aalborg University.

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IONUT TRINTIS,

Aalborg, September 2012

To Ancuta
To our Families

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Nomenclature

Abbreviations

AC	alternating current
DC	direct current
DC-DC	DC to DC converter
DC-AC	DC to AC converter
HV	high voltage
LV	low voltage
IGBT	insulated gate bipolar transistor
IGCT	integrated gate commutated thyristor
VSC	voltage source converter
CHB	cascaded H-bridge
ChB	cascaded half-bridge
ANPC	active neutral point clamped
NPC	neutral point clamped
ARCP	auxiliary resonant commutated pole
FC	flying capacitor
DAB	dual active bridge
FIT	failure in time
BESS	battery energy storage system
SOC	state of charge
DOD	depth of discharge
PLL	phase-locked-loop
QSG	quadrature signal generator
SOGI	second order generalized integrator
SRF	synchronous reference frame
PNSC	positive negative sequence calculator
I	integrator
PI	proportional integrator
PR	proportional resonant
DPC	direct power control
PWM	pulse width modulation
SVM	space vector modulation

Contents

PS	phase shift
LS	level shift
SHE	selective harmonic elimination
THD	total harmonic distortion
PF	power factor

Symbols

t	time
f	frequency
ω	angular frequency
v	voltage
i	current
θ	angle
L	inductance
C	capacitance
R	resistance
Q	electric charge
s	complex number
p	active power
q	reactive power
f_p	active power slope
f_q	reactive power slope
ψ	error
k_p	proportional gain
k_i	integral gain
S^*	switching function / duty cycle
S	power electronic switch

Subscripts

g	grid side
c	converter side
DC	DC side
α, β	stationary frame
dq	rotating frame
res	resonant
h	harmonic order

Superscripts

$+$	positive sequence
$-$	negative sequence
$*$	imposed / reference

Chapter 1.

Introduction

1.1. Background and motivation

The necessity to reduce the harmful emissions from the conventional power plants, leads to a transition of the power systems towards dispersed generation production based on renewable energy sources. Wind power and photovoltaic installations are the most important renewables with significant worldwide installed capacities and high annual growth rate. The drawback of this renewable energy sources is the high fluctuation on daily and seasonal basis. This fact makes their integration with high percentage into the grid a well-known challenge, since the security of supply is a high priority [1]. This can be deduced from Fig. 1.1 which shows the wind power production and demand in Denmark West for 20% wind in 2008 and the scaling to 50% for 2025 [2].

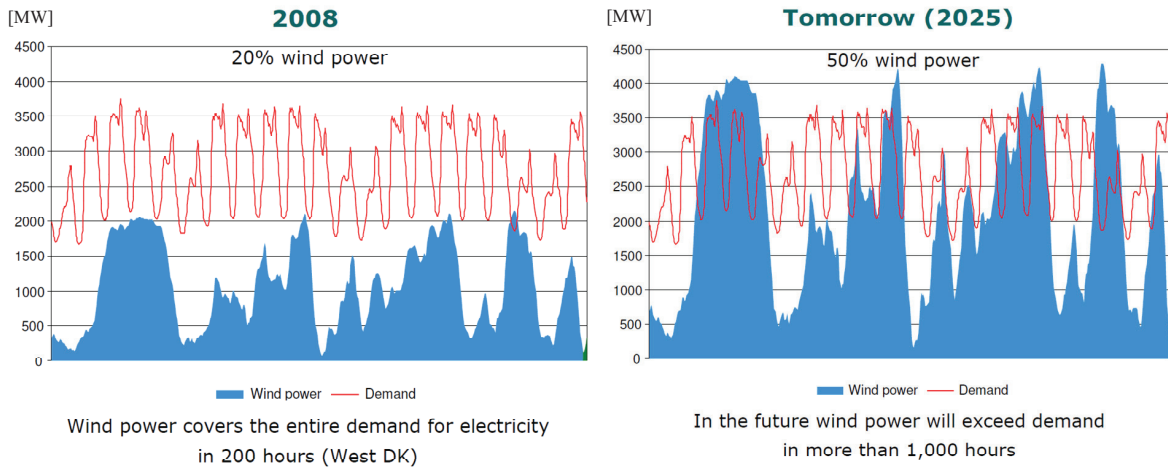


Figure 1.1.: Wind power production and demand for Denmark West [2]

One way to overcome this drawback is to strengthen the electrical network. However, this implies high expenses and the overall efficiency drops when the energy is transported over long distances [3]. Moreover, the grid codes for different interconnected countries must be unified and this is a long time task [4]. Another way is to install distributed energy

storage units. Using communication between generators, loads and storage systems, the high level control can define groups that can operate independent or together with the main electrical grid and can behave similar to a conventional power plant [5, 6]. The generation-consumption can then be optimized by using minimization criteria for the given priority (lowest price, highest efficiency, lowest CO₂, etc.). Stationary energy storage is a complementary solution, which can be optimized for different kind of services provided. In Fig. 1.2 the potential applications for energy storage are shown, and the state-of-the-art storage technologies are presented in Fig. 1.3 [7].

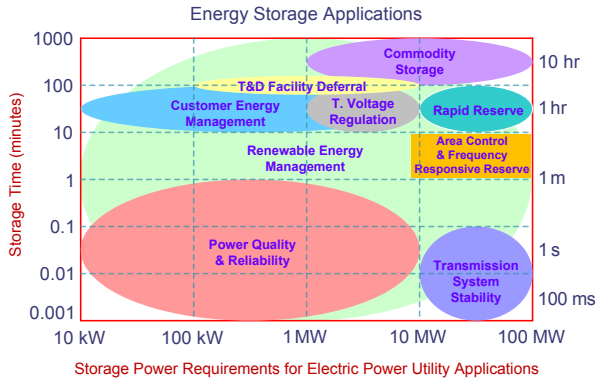


Figure 1.2.: Storage Applications

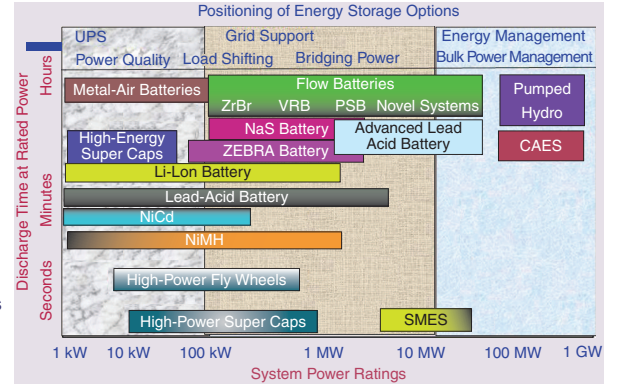


Figure 1.3.: Storage Technologies [7]

As an energy storage solution with timing for few seconds up to several hours, with capacities up to 100 MWh and fast response, batteries are a suitable and efficient solution [8, 9]. However, today's investment price in the battery system is high and is difficult to build storage systems that can be economically self sustained. In Fig. 1.5 the cost of Lead-acid, Li-ion, NiCd and NiMH battery technologies is shown [10]. Today's price is the high value on the given variation, and the expectancy of price drop being the low investment price [10, 11, 12, 13].

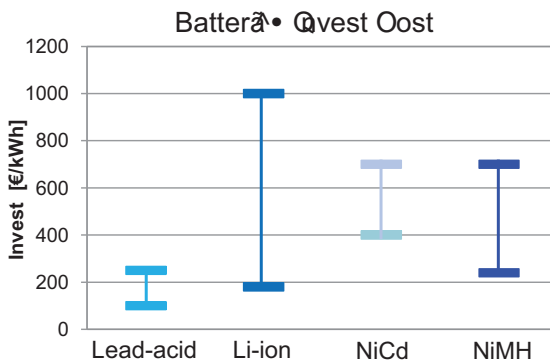


Figure 1.4.: Batteries investment cost

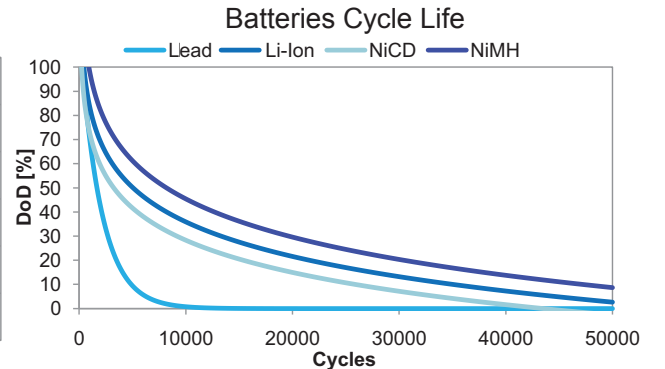


Figure 1.5.: Batteries lifetime as $f(\text{DOD})$

The batteries lifetime dependency on depth of discharge (DOD) is shown in Fig. 1.5. Moreover, the calendrical lifetime must also be considered. This is around 5 years for

Lead-acid and NiCd, 10 years for NiMH and 15 years for Li-ion. Therefore, for the given operation scenario the planned cycling lifetime has to match the calendric life for the best system economical outcome.

Even if the energy storage in batteries is still an expensive solution nowadays, the outlook of the future vehicle-to-grid opens new perspectives for centralized storage systems such as enabling the reuse of electric cars batteries with reduced capacity before recycling. Thus, the development of centralized storage systems is needed for the future grids and will coexist with distributed energy storage systems.

The connection of storage systems can be done at different voltage levels, depending on the application scenario. For increased power and energy ratings, it is natural to increase also the connection point voltage and reduce battery and converter current ratings. It was shown that high efficiency can be achieved with increased nominal voltage of the battery system [14]. Medium voltage is an appropriate level where both transmission and distribution networks can take support from the storage system [15]. At this level, multilevel converters are employed as grid interface, making use of conventional and mature power electronic devices.

In the design of the power electronic converters for battery energy storage, it is critical that the charging and discharging procedures are implemented in such a way that it will enhance the battery lifetime. External stress factors are not desired, since already the battery system is the technology with the smallest lifetime and expensive.

1.2. Objectives

The project this work is based on was financed by E.ON AG [16] under the E.ON Research Initiative under the call on Energy Storage with the project 2007/B4-HIGHLY EFFICIENT AND RELIABLE MODULAR BATTERY ENERGY STORAGE SYSTEMS (HERMES) in cooperation with RWTH Aachen University, Germany. The aim of the project was to design a modular battery energy storage system, taking into account the interaction between the electrochemical system and the power electronics. The project main objective was to identify the optimum battery building block for grid applications with large-scale potential having the rated power in the MW range and energy capacities from 1 second to 12 hours. To achieve this objective, a 6 kV battery energy storage test bench was to be realized to prove a potential large-scale battery concept.

The first objective of this work was to realize a custom grid connected DC-AC converter to be used in the HERMES test bench. The rated power is 100 kW and the control should be as active rectifier, to allow a connection with a current controlled DC-DC converter as battery charger/discharger.

To connect a 6 kV battery system to the power grid, a power electronic interface has to be designed. Therefore, another objective was to make a survey on suitable medium-voltage

multi-level converter topologies including soft-switching topologies for high efficiency. Converter topologies design and loss analysis was a following objective, to determine the amount of active and passive components required.

The knowledge of high voltage battery systems ($V_n > 1\text{ kV}$) is still limited nowadays. Their safety, efficiency, reliability and feasibility are not well known. Therefore, another objective of this work was to design power electronics that can allow a connection to the medium voltage grid using batteries with low voltage ratings which are at technological maturity to date.

1.3. Methodology

In the realization of the DC-AC converter to be used in the HERMES test bench, the 110 kW Danfoss VLT FC 302 a low voltage two-level converter which is commercial product from Danfoss A/S [17] was modified and interfaced using the IPC2 interface and protection card developed at Aalborg University [18]. The control structures were simulated in MATLAB/Simulink [19], and the controllers were designed either via analytical calculations or using the Control System Toolbox from MATLAB.

Control implementation for the HERMES grid converter was realized on a XCS 2000 AIX Control System, control platform comprising of a field programmable gate array (FPGA) and two digital signal processors (DSP) [20]. Additional interface printed circuits boards (PCB) were designed using Altium Designer [21]. Testing of the grid converter functionality has made use of a 30 kW, 1000 V power supply to emulate the batteries and DC-DC converter.

Control structures, multilevel converters switching models and power electronic devices loss models were implemented in MATLAB/Simulink using the PLECS blockset [22].

1.4. Limitations

One of the limitation during the development of the low voltage DC-AC grid converter, was the DC power supply that was used to emulate the test bench batteries and DC-DC converter, which was limited in power up to around 22 kW for an output voltage of 750 V. Therefore initial tests were done only at light load. Another related limitation was the weak grid at the connection point during tests. The high impedance of the grid, and the light load operation, has created difficulties in the tuning of the harmonic compensation for the current control.

The definition of the optimal building block of the HERMES system was one of the main limitations of the project. Having undefined parameters of the battery systems has led to a more general approach considering the power electronics. The design of converter

topologies that can accommodate a large variety of battery technologies and for different battery voltage levels was necessary.

The laboratory implementation of the modular converters that were proposed during the project was not finalized. This was mainly because of the time frame of the project and also because of the chosen software implementation based on distributed processing units. Therefore, it was not possible to present experimental results for those converter topologies.

1.5. Scientific Contributions

The main scientific contributions of this work, from the author's perspective, are outlined in the following:

- A new modular multilevel converter with integrated energy storage.
A two stage cascaded converter topology with construction based on half-bridge converter legs was introduced. This structure can interconnect a DC and AC grid with bidirectional power flow, where both can be backed-up with the distributed energy storage units installed in each converter cell. This converter topology has low dependency on the energy storage unit characteristic, and is suitable for medium and high voltage grids.
- Two-stage cascaded H-bridge converter for energy storage.
The connection of low voltage batteries to the 4.16 kV medium voltage AC grid was proposed to be realized with the cascaded H-bridge converter with bidirectional boost converters. This is also a modular concept, and the design and control was investigated. A novel control strategy was proposed to fit the requirements of this converter topology.
- Case study on single-stage medium voltage converters for storage.
The high efficiency can be achieved with a single stage conversion system. However, the converter operation is highly dependent on the energy storage characteristic, fact that is challenging in the converter design and control. An investigation has been done, for a design case scenario, where different converter topologies were compared.
- A survey on medium voltage multilevel converters.
This contribution can inspire further research on multilevel converters, for different applications that require highly efficient and reliable design. Hard-switched and soft-switched topologies were reviewed, identifying their advantages and disadvantages.
- A survey on control methods for grid connected converters.
A state-of-the-art in synchronization, current control and DC voltage control was

presented. This contribution can inspire further research on new and emerging control structures for grid converters.

1.5.1. List of Publications

- Ionut Trintis, Stig Munk-Nielsen, Remus Teodorescu, "A new modular multilevel converter with integrated energy storage", *37th Annual Conference of the IEEE Industrial Electronics Society (IECON 2011)*, Melbourne, AU, 2011
- Ionut Trintis, Stig Munk-Nielsen, Remus Teodorescu, "Cascaded H-bridge with bidirectional boost converters for energy storage", *14th European Conference on Power Electronics and Applications (EPE 2011)*, Birmingham, UK, 2011
- Ionut Trintis, Stephan Thomas, Tobias Blank, Christoph Roggenendorf, Stig Munk-Nielsen, Remus Teodorescu "Bidirectional converter interface for a battery energy storage test bench", *14th European Conference on Power Electronics and Applications (EPE 2011)*, Birmingham, UK, 2011
- Tobias Blank, Stephan Thomas, Christoph Roggenendorf, Thomas Pollok, Ionut Trintis, Dirk Uwe Sauer, "Design and construction of a test bench to characterize efficiency and reliability of high voltage battery energy storage systems", *International Telecommunications Energy Conference (INTELEC 2010)*, 6-10 June, Orlando, US, 2010
- Ionut Trintis, Stig Munk-Nielsen, Remus Teodorescu, "Single stage grid converters for battery energy storage", *5th International Conference on Power Electronics, Machines and Drives (PEMD 2010)*, 19-21 April, Brighton, UK, 2010
- Christoph Roggenendorf, Tobias Blank, Stephan Thomas, Ionut Trintis, "Design and Construction of a Test Bench to Characterize the Charging and Discharging Behaviour of Batteries in High Voltage Storage Systems", *4th International Renewable Energy Storage Conference (IRES 2009)*, 24-25 November, Berlin, DE, 2009

1.6. Outline

The work is divided in two parts. The first part is on CONTROL OF DC-AC GRID CONVERTERS and contains two chapters (2 and 3). The second part is on MEDIUM VOLTAGE GRID CONVERTERS FOR ENERGY STORAGE and contains four chapters (4, 5, 6, 7). A summary, conclusions and future work is given in chapter 8. Two appendices are on SPACE VECTOR TRANSFORMATIONS and POWERS AND SEQUENCES CALCULATION.

CHAPTER 2 shows a review of the state-of-the-art control structures for grid converters. This includes phase-locked loop systems for single and three-phase, linear and nonlinear current control methods and DC voltage control.

CHAPTER 3 shows the implementation of a low voltage two-level active rectifier to be used in a high voltage battery energy storage test bench. The interaction with the current controlled DC-DC converter is also simulated. Finally, the experimental results for the DC-AC grid converter and for the operation of the entire test bench are shown.

CHAPTER 4 presents the state-of-the-art on medium voltage multilevel converters. Hard-switched and soft-switched converter topologies are shown for the most promising configurations. Advantages and disadvantages are given for each converter topology and finally the component count is summarized.

CHAPTER 5 analyses four multilevel converters to be used for direct connection of battery systems to the medium voltage AC grid. A comparison is realized over a 25% battery voltage variation considering the semiconductors requirements and losses, output voltages and harmonic distortion.

CHAPTER 6 presents the design and control of a two-stage cascaded H-bridge converter as interface for modular low voltage batteries to the medium voltage grid. The independent phase control for the DC voltages and AC currents is proposed and validated by simulation. In final, a loss analysis is performed over the entire battery voltage variation.

CHAPTER 7 introduces a new modular converter concept with integrated energy storage. Converter operation and control methods are presented, and the identified operation modes are simulated to validate the possible power flows. Finally, an implementation concept for a complete modular energy storage system is given together with some design considerations.

Part I.

Control of DC-AC Grid Converters

Chapter 2.

State-of-the-Art on Control for DC-AC Grid Converters

This chapter gives a brief description of the state of the art control methods for grid connection of DC-AC converters

2.1. Introduction to Grid Control Structures

The control of DC-AC grid converters started its development almost a century ago, when the first power converters based on mercury arc devices were developed to interconnect two grids with different voltage and frequencies [23, 24]. From its early stage, it was possible to apply different control methods - constant power or variable power with respect to the grid frequency.

Nowadays with the development of power semiconductors devices, converter topologies and digital signal processors, the control structures enable the control of active and reactive powers and their sequence as well as the harmonic content of the transferred currents. Fig. 2.1 shows the block diagram of the grid control structure.

A synchronization method is used to detect the phase angle of the grid voltage, which can be used for coordinate transformations to and from the dq frame (Sec. 2.2). Frequency and voltage band controls are ancillary services that the converter can provide, through the control of active and respectively the reactive currents, with limitations to its rated power. Whenever the converter is to be operated as active rectifier the DC-link voltage is controlled, reacting on the converter active current reference (Sec. 2.4). The current control is the core of the grid converter's control structure, its operation shaping the performance of the complete system [25, 4] (Sec. 2.3). This is the closed-loop with the highest bandwidth and it has to provide high dynamic response, reduce the output current harmonic distortion or it must control specific harmonic frequencies in case of active filtering [26]. Finally, the modulation strategy is the converter's topology dependent open-loop algorithm which converts the reference voltage into discrete steps to achieve the desired output voltage after filtering.

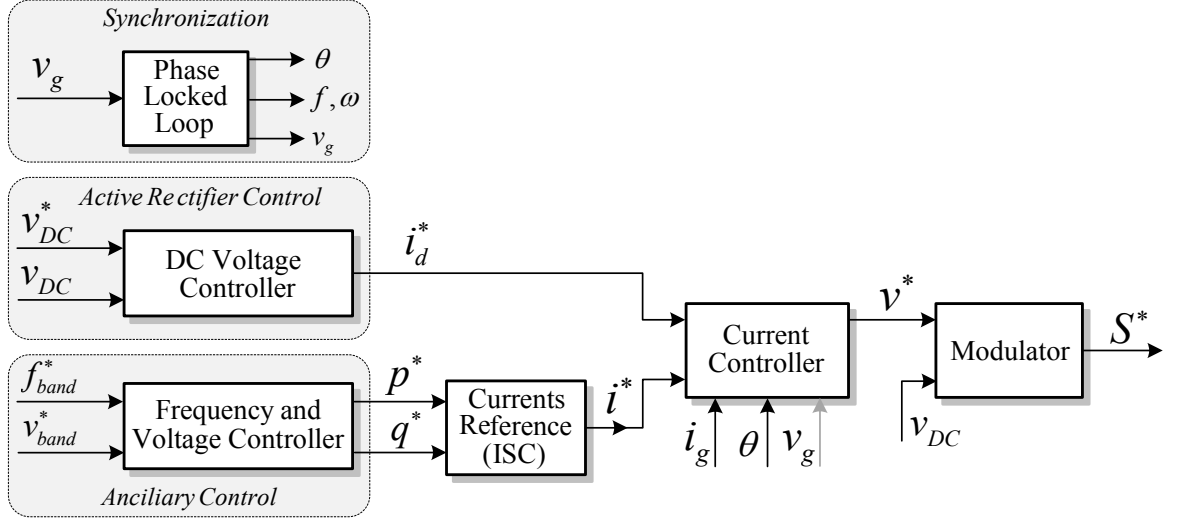


Figure 2.1.: General control structure of DC-AC grid converters

In the following, a review of the state of the art control structures is presented. The ancillary control strategies (f and v control) are not considered in this work, since it is a service dependent on the converter power ratings and dependent on the application. Modulation strategies are also not discussed in this chapter, these being dependent on the used converter topology and current controller. For linear current control methods however, a pulse width modulation (PWM) strategy is considered to generate the duty cycles based on the input voltage references.

2.2. Synchronization Methods

The grid converter's synchronization with the grid voltage is one of the key methods that are mandatory to be used. It is critical to detect the correct phase angle of the grid voltage, to allow a safe and smooth connection and to be able to inject/draw the desired currents. Phase-Locked-Loops (PLL) are the most popular methods used nowadays, introduced in 1923 [27] with the first patent from 1932 [28]. In Fig. 2.2 the general PLL structure is shown, consisting of a Phase Detector (PD), Loop Filter (LF) and a Controlled Oscillator (CO).

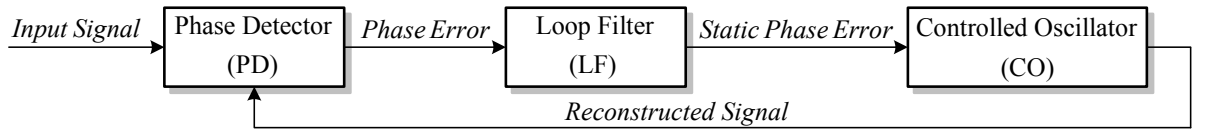


Figure 2.2.: Phase-Locked-Loop General Structure

The role of the PD is to generate the phase error between the actual input signal and the internal reconstructed signal. The phase error is then filtered by the LF, output used to reconstruct the signal with the CO. First implementations were realized with analog circuits, the PD being implemented with a multiplier, the LF with a RC low-pass filter and the CO with a variable capacitor to control its resonant frequency based on the input bias voltage. Nowadays, the PLL as well as the control implementation is discretized and implemented in digital signal processors (DSP), where the LF is a PI controller and the CO is an integrator usually with a feed-forward term in the input.

Depending on the input signal(s), adaptation of the PD module results in a classification of the PLL methods in three-phase (see Sec. 2.2.1) and single-phase (see Sec. 2.2.2) PLL's. With the development of methods for generating the virtual β component from a phase voltage [29], basically the single-phase PLL becomes a particular case of the three-phase PLL. This is used in single-phase systems or in particular three-phase systems with independent phase voltage synchronization and control, see application in Sec. 6.3.

2.2.1. Three-phase methods

Three-phase synchronization methods can be classified in open-loop and closed-loop. One of the simplest synchronization technique is to transform the input three-phase voltages in $\alpha\beta$ or dq frames (see A1), filter out the harmonics and calculate the angle from the $\alpha\beta$ frame using the inverse tangent function [30]. However, the operation during voltage frequency deviations requires adaptation of the resonant filters and the behaviour during unbalanced input voltages is poor. Another proposed structure is based on Kalman filtering algorithms [31], structure which provides good accuracy under distorted and unbalanced input signals. The disadvantage is the high required processing power as well as selecting the optimal covariance matrices [32].

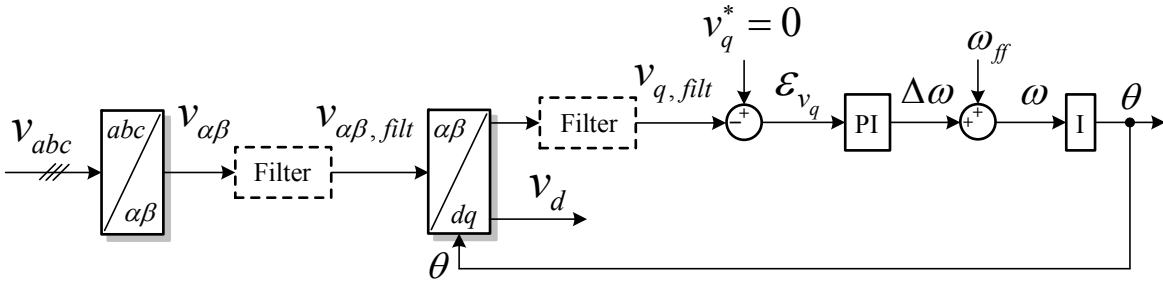


Figure 2.3.: Three-phase PLL general structure

The widely accepted and used synchronization method for three-phase systems is presented as a general structure in Fig. 2.3, the dq -PLL also known as the synchronous reference frame PLL (SRF-PLL). The three-phase quantities are transformed in the dq frame using the estimated phase angle, and the phase angle error is reflected in the alignment

on the q axis of the voltage vector. This phase angle error is regulated by the PI controller to zero, and the PI tuning (usually done with the *symmetrical optimum* [33]) defines the PLL dynamic performance.

The basic structure implemented without the filtering blocks, works well on balanced and light distorted grid voltages. However, in a case of a grid fault or transients of high power electronics, the grid voltages may be highly distorted and unbalanced and the SRF-PLL cannot detect the correct grid voltage phase angle.

To mitigate the distortion, filtering either on the $\alpha\beta$ frame or on the dq frame can be implemented. Basically with the decrease of the bandwidth of the PI controller, a natural low-pass filtering can be achieved with the disadvantage of overall PLL slower dynamics.

The grid voltages filtering on the $\alpha\beta$ frame based on the Second Order Generalized Integrator (SOGI) is a solution with theoretical no delay. The Double SOGI PLL (DSOGI-PLL) structure was introduced in [34], presented in Fig. 2.4. For grid control structures where only the control of positive sequence currents is desired, distortion immunity is required, the DSOGI-PLL represents a reliable synchronization solution at a relatively small computation cost.

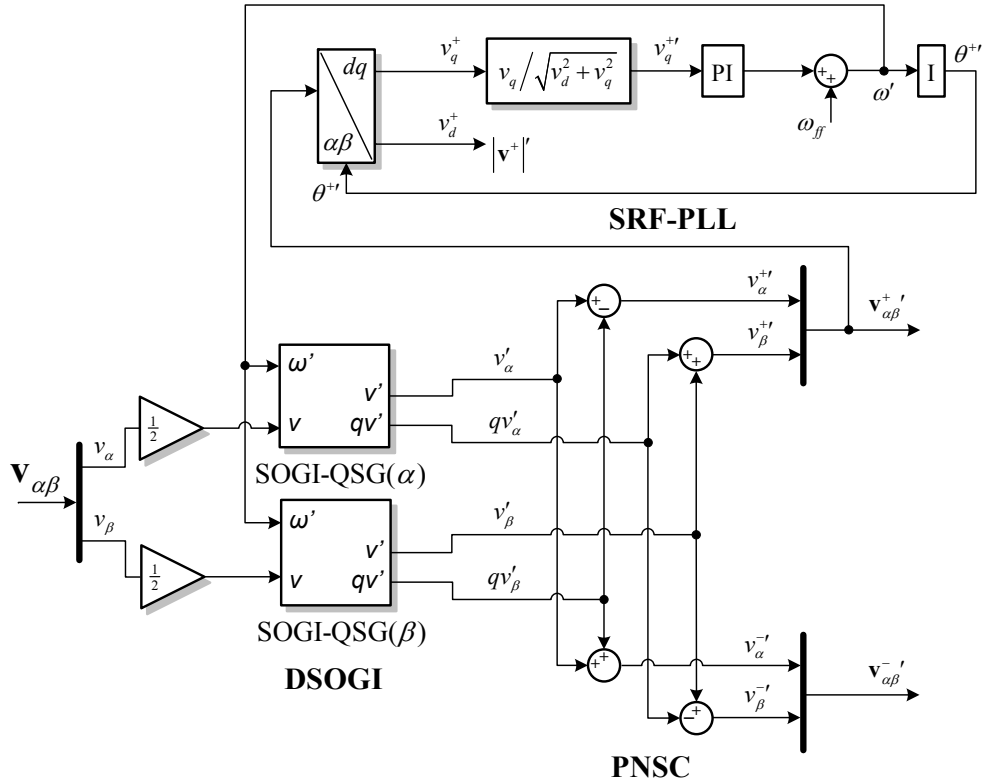


Figure 2.4.: Double SOGI Phase-Locked-Loop algorithm [34]

The core of the filtering algorithm on the $\alpha\beta$ components of the grid voltage is the SOGI Quadrature Signal Generator (SOGI-QSG) [35], see Fig. 2.5. At a given input signal, this block has a theoretical infinite gain at the given angular frequency ω . Therefore it is possible to extract from the input signal only the desired frequency components, like the fundamental component of the grid voltage. Moreover, the output of the second integrator is the filtered output signal with a 90° phase shift delay called in quadrature signal [36] or orthogonal signal [35]. Therefore, the output of the SOGI gives the filtered input signal which can be aligned on the α axis on the stationary frame ($\alpha\beta$) and the quadrature signal can be aligned on a virtual β axis. Having this, the grid voltage $\alpha\beta$ components can be decoupled in positive and negative sequence by the Positive Negative Sequence Calculator (PNSC) shown in Fig. 2.4.

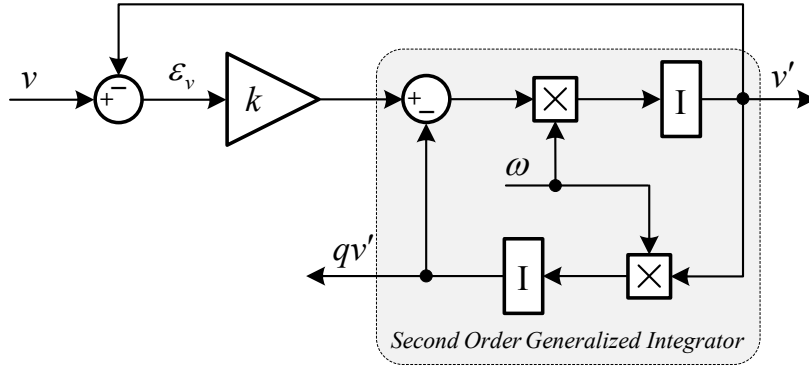


Figure 2.5.: Quadrature Signal Generator based on SOGI (SOGI-QSG) [35]

To be able to extract the correct grid voltage angle under unbalanced condition the decomposition of the positive and negative sequences of the grid voltage is required. This is achieved using the instantaneous symmetrical components (ISC) method [37]. Based on the ISC decomposition of the grid voltage it is possible to synchronize only with the positive sequence of the grid voltages, and the Decoupled Double Synchronous Reference Frame PLL (DDSRF-PLL) was introduced [38, 4]. Having also the magnitudes of the positive and negative sequences of the grid voltage, given by this structure, it is possible to inject/draw also unbalanced currents to reduce the power system oscillations [4]. However, the structure presented in [38] is not feasible under a highly distorted grid.

New synchronization methods were introduced recently, the locked-loop being realized on the grid frequency rather than on the grid phase angle, such as: Adaptive Notch Filter (ANF) [39], DSOGI Frequency Locked Loop (DSOGI-FLL) [40, 36]. This synchronization methods are claimed to present increased robustness [36], and may bring benefits in control structures based on $\alpha\beta$ frame [4].

2.2.2. Single-phase methods

First developed synchronization methods were designed for independent sinusoidal signals [27], used also nowadays with basically the same structural building blocks. Research and development has led to improvements in the synchronization performance, optimizing the performance for the specific application. Several methods are available to be used, in open-loop or closed loop. Synchronization in open-loop is usually based on filters, from which we can distinguish the following methods: discrete Fourier transform (DFT) [31], weighted-least-square-estimation (WLSE) [41], adaptive notch filter (ANF) [42], Kalman filtering [31] and artificial neural networks (ANN) [43]. Closed-loop synchronization methods are based on PLL from which various methods were proposed with particular PD implementations: Enhanced PLL (EPLL) [44], Adaptive PLL [45] and in quadrature signal generation (QSG) based PLL's. The QSG-PLL is in fact a particular implementation of the SRF-PLL adapted for single-phase systems, with the general structure shown in Fig. 2.6.

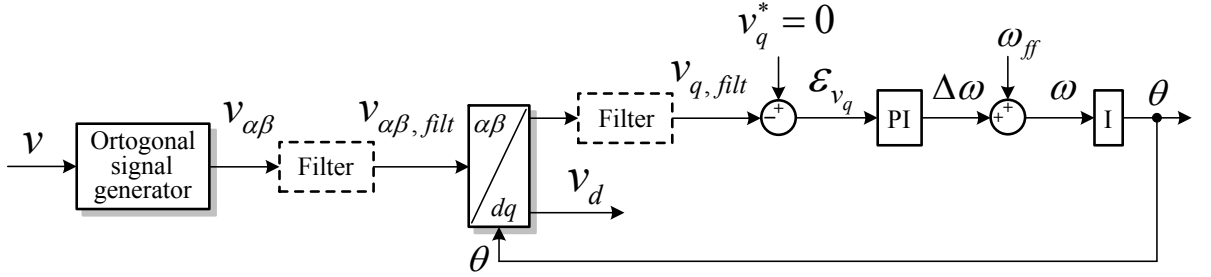


Figure 2.6.: Single-phase SRF-PLL general structure

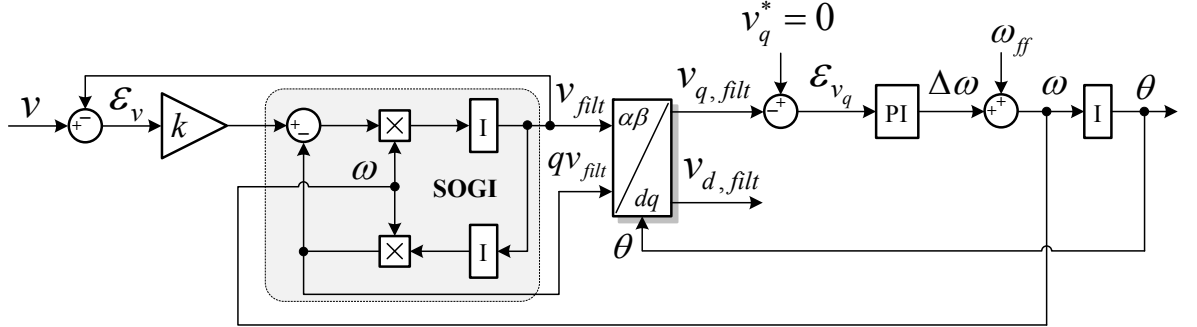


Figure 2.7.: Single-phase SRF-PLL based on SOGI-QSG

Different solutions can be adopted for the quadrature signal generation on the voltage to be synchronized with, such as: T/4 Transport Delay, Hilbert Transform, Inverse Park Transform, Generalized Integrator (GI), Second Order Generalized Integrator [4], D-filters based [46] and Kalman filter based [47]. The first three methods do not ensure filtering and therefore in Fig. 2.6 a filter needs to be employed either on $\alpha\beta$ or dq frames.

The Kalman filter-based method requires variable sampling time to correct the errors due to frequency deviations, fact that may not be allowed by the digital implementation platform. The GI, SOGI and D-filter based methods however, apart from generating the in quadrature signal provides also filtering at the tuned frequency and are frequency adaptive. Therefore, implementing one of these structures the optional blocks from Fig. 2.6 can be disregarded. Fig. 2.7 shows the structure of the single-phase SRF-PLL based on SOGI-QSG, structure which is applied in Sec. 6.3.

2.3. Current Control Methods

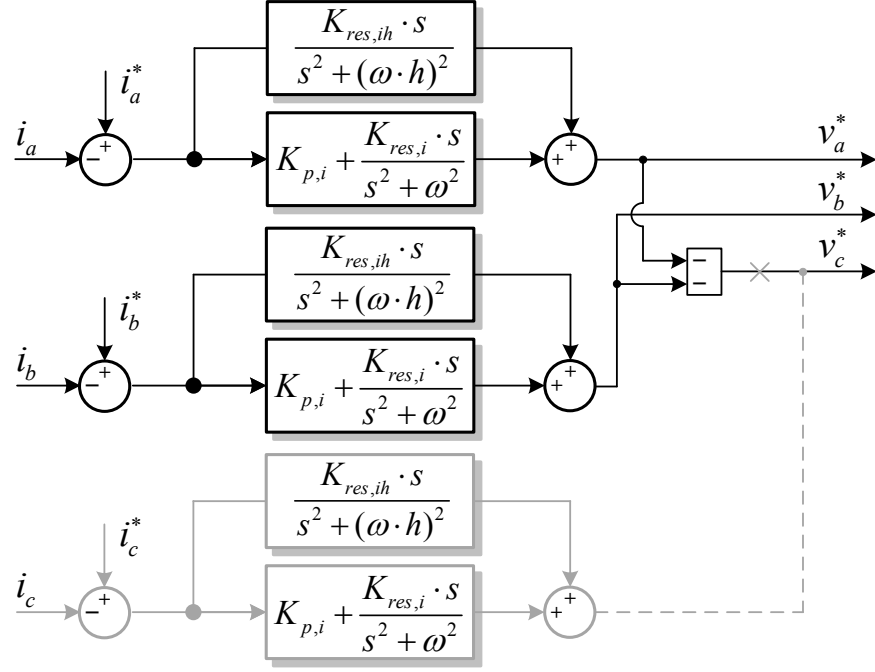
The grid converter's current control method is the core of the control structure, its performance being critical for the dynamic response, operation during grid faults and output current distortion to comply with the grid connection requirements [4]. The basic function is to control the current in the output filter (L or LCL) to the desired reference, by modulating the available DC-link voltage. Many current control concepts were proposed over the time, linear and non-linear, with advantages and disadvantages which are selected and applied for different applications. Linear controllers are based on PWM modulation using proportional resonant (PR) controllers or deadbeat controllers in the natural abc frame or the stationary $\alpha\beta$ frame, or PI controllers in the dq rotating frame. Non-linear controllers are based on PWM such as passivity based control (PBC), or on ON-OFF control such as hysteresis and predictive control with minimization criteria.

2.3.1. Natural frame

The current control in the natural abc frame requires controllers that can compensate effectively the error of sinusoidal signals, and adapt with the frequency change [48, 49, 50, 51]. The structure using PR controllers to regulate the error on the fundamental frequency, introduced in [48], is shown in Fig. 2.8. To eliminate the harmonic content of low order harmonics, resonant integrators are tuned at the required frequencies [50].

Two controllers are normally required in a three-phase system, when regulation of the currents is done symmetrically. Whenever it is desired to control the currents independently, a third controller can be employed [52]. It was shown that it is possible to control the active and reactive power without the use of any transformation from the dq frame, using the structure from Fig. 2.8 in combination with the single phase PLL structure from Fig. 2.7. However, the plant of the three-phase load/source is not decoupled in single phase systems and therefore the control of the three phases must be done coordinated with respect to phase shifts and injected/drawn currents sequence [4].

Current control implementation using PI controllers in abc frame was one of the first used methods [53]. Because of the steady state error, implementations were done in dq frame. However, it was shown that the PI current controller can be used in the


 Figure 2.8.: Natural frame abc current control with PR controllers

abc frame with very good transient and steady state performance, if it is enhanced with PWM transport delay compensation [54]. The steady state error is not removed, but the reference tracking is accurate and with improved transient response.

Another type of controller which can be used in the abc frame is the deadbeat (DB) controller. It is a linear predictive controller introduced in 1973 [55] and firstly used in power electronics in 1985 [56], also called *One Sample Ahead Controller*. It predicts the current error on the next sample based on current and previous measurement, and generates the duty cycle to eliminate the error at the end of the next switching period. The prediction however, is based on the plant model and therefore is highly sensitive to parameters change. To overcome this drawback, the artificial decrease of the controller constant term in its transfer function leads to an increased damping [57] and therefore allowing the operation over a wide parameter change in the plant (L or LCL filter).

2.3.2. Stationary frame

Transforming the feedback currents from the natural abc frame to the stationary $\alpha\beta$ frame, using the Clarke transformation (see A1→Eq. 1), regulation of the three-phase currents can be done using two sets of controllers. Compared with the natural abc frame, the same computation burden is required when indirect control of the third phase is done. It must be noted that in the $\alpha\beta$ frame the controllers of the two in quadrature α and β , have both a direct influence on all three phases. The control structure using PR

controllers for fundamental and harmonics compensation is shown in Fig. 2.9. The zero sequence component is not considered, because normally there are no zero sequence produced currents in the three-phase system with isolated neutral [58].

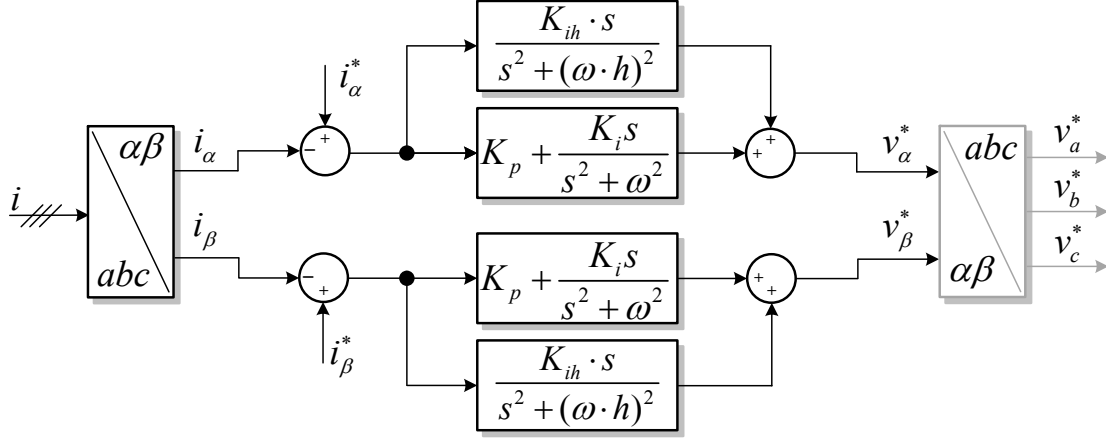


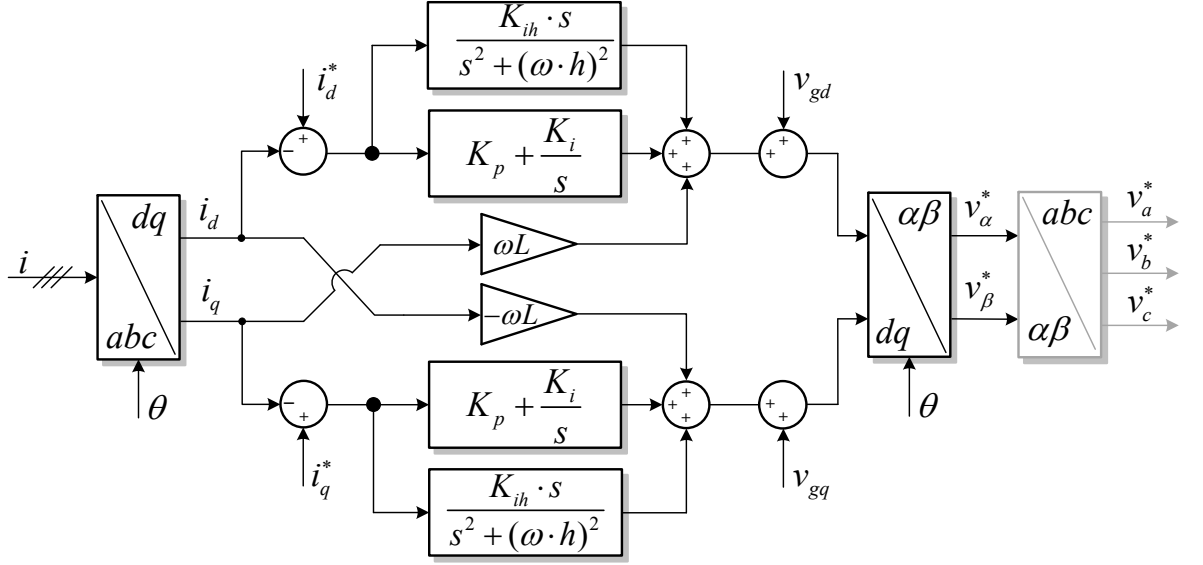
Figure 2.9.: Stationary frame $\alpha\beta$ current control

Under unbalanced grid condition, the control of the positive and negative sequence currents with this structure can be achieved [50], only by having the two sets of controllers from Fig. 2.9. Generation of current references has a major influence on the current control performance [59]. Whenever the current references are given in d and q components and transformed in $\alpha\beta$ frame, rotated with the PLL angle of the positive sequence, only the positive sequence error is compensated.

2.3.3. Rotating frame

One of the most used control techniques in control of electrical machines and grid connected converters is the rotating dq frame control, also called voltage oriented control. The use of PI controllers to control three-phase AC currents cancelling the error of two in quadrature DC currents (dq) is made possible by using the Park transformation (see A1→Eq. 3). The steady state error is brought to zero [60] since the classical integrator has infinite gain at zero frequency, and the performance is similar to a resonant control in stationary frame [49]. The particularity of the dq frame control is that due to the rotation with the angular frequency ω , the resulting d and q components are coupled in the converter model [61]. Therefore a decoupling network is necessary to be implemented, see Fig. 2.10, to decouple the two PI controllers actions on the two axis. However, the decoupling is not ideal since the plant inductance is not known precisely.

Feedforward of the dq components of the grid voltages is required to minimize the effort in the PI controllers, as shown in Fig. 2.10. When the grid voltages are distorted, filtering is necessary to deliver a clean reference for the PWM modulator.


 Figure 2.10.: dq current control

Regarding harmonic compensation in dq frame, it can be implemented using resonant integrators tuned between two compensating frequencies ($h + \omega$ and $h - \omega$) [62, 63, 64] (eg. 6^{th} , 12^{th} , 18^{th}). This is valid in the case of compensating the harmonics generated by diode rectifiers, having for instance in stationary frame negative sequence 5^{th} harmonic and positive sequence 7^{th} harmonic which rotated with ω in dq frame results in negative and positive 6^{th} harmonic. This results in a reduced number of used resonant integrators for harmonic compensation.

The compensation for the fundamental frequency is done only for the sequence that is used to rotate the abc components, which usually is the positive sequence. For control of the negative sequence currents, if necessary in case of faults, another set of controllers is required with two more transformations. Moreover, the second harmonic filtering is necessary due to the power oscillations given in this case (see A2→Eq. 10,11).

2.3.4. Hysteresis

Hysteresis control is a type of nonlinear control based on ON-OFF controllers for each phase, structure shown in Fig. 2.11. Each controller reacts to the measured current, and keeps the error in the hysteresis band as shown in Fig. 2.12 [65]. Thus, the maximum phase current error is equal to half the hysteresis band h , the maximum line current error is $2h$ and maximum current vector error is $4h$ [53].

The operation of hysteresis current control is inferior to PWM based control at low modulation index due to the required high switching frequency. However, grid connected converters operate at high modulation indices all the time. The advantages in the basic

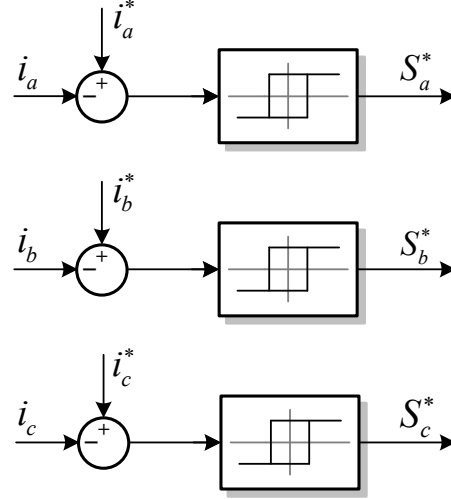
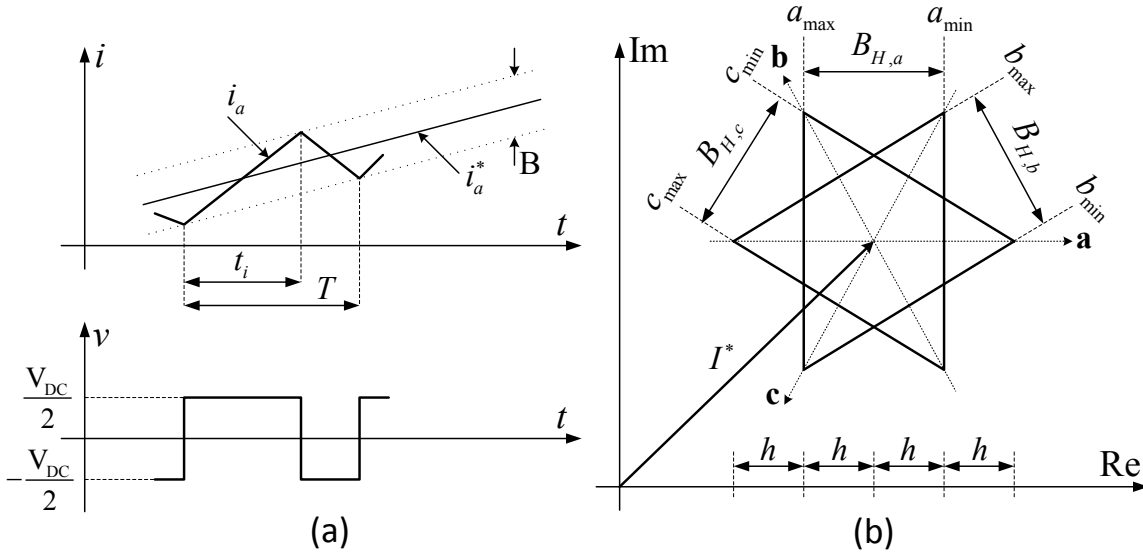


Figure 2.11.: Hysteresis current control

Figure 2.12.: (a) Phase a current regulation; (b) Hysteresis bands for phases abc

implementation are: high dynamic performance, control and implementation simplicity, and independence of the load parameters give robustness. One of the disadvantage is the stringent requirements on the current sensing, which directly influences the controller performance. The current measurement must be noise-free, and if the control is implemented in a processor the sampling frequency and resolution of the analog to digital converter must be high.

The main concern of the hysteresis control technique is the variable switching frequency. The operating switching frequency is also influenced by the coupling between phases,

where the error of the three-phase current vector is high (see Fig. 2.12.(b)). Operating the converter at variable switching is not desired, especially for high power, because of the spread harmonic spectrum. Therefore, work has been done to reduce the interaction between phases by using adaptive hysteresis bands in order to achieve constant switching frequency [66, 67]. This however increases the control complexity, but the dynamic response and robustness is not affected.

2.3.5. Direct power control

The principle of controlling indirectly the grid currents by controlling the instantaneous active and reactive powers was introduced in 1991 [68], with the basic control structure shown in Fig. 2.13. Two hysteresis controllers are used to control the active and reactive power, and the switching table selects the appropriate voltage vector with the sector given by the grid voltage angle. Advantages like no coordinate transformation, no required decoupling in the control of active and reactive powers, and the fast response makes this control strategy very attractive.

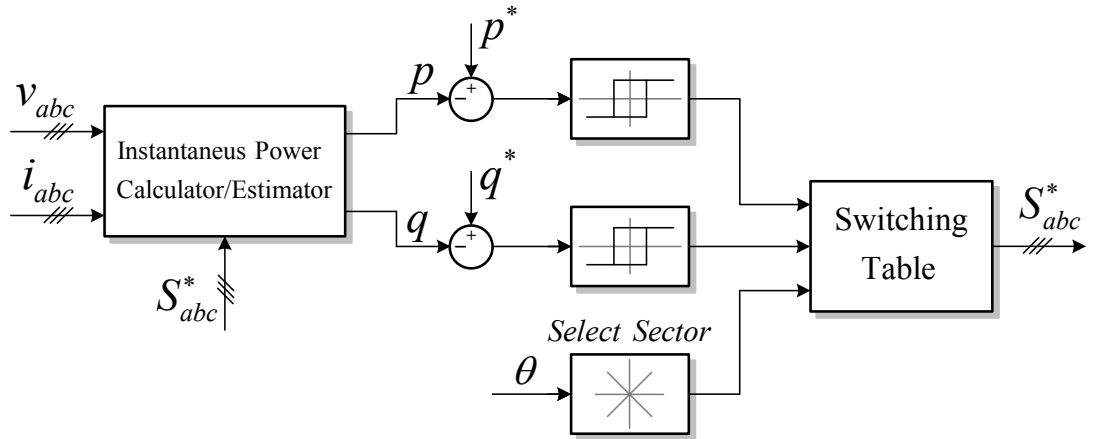


Figure 2.13.: Direct power control structure

Based on the same principle, control structures were introduced to implement the control with reduced number of sensors, by using estimators [69, 70]. Measuring only the converter's output currents, the direct power control (DPC) can be implemented by estimating the grid voltages and the instantaneous output/input powers [69]. Looking at the power grid as to a virtual generator, another DPC method was developed based on the estimation of the virtual flux, this being used to calculate the instantaneous powers [70]. However, the disadvantages of the hysteresis controller such as requirement of high sampling frequency and variable switching frequency and are still present. To compensate for this drawbacks, the direct power control using space vector modulation (DPC-SVM) was introduced in [71], shown in Fig. 2.14.

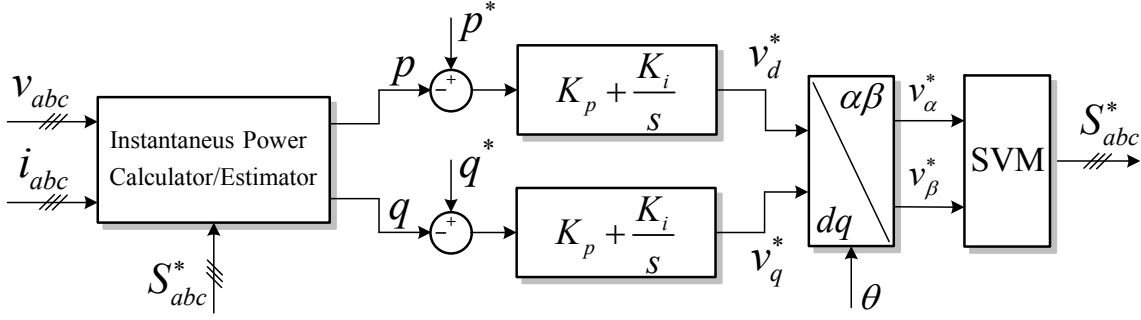


Figure 2.14.: Direct power control based on SVM

In the DPC-SVM, the active and reactive powers are regulated using PI controllers which give the voltage references in the dq frame. Therefore, an additional dq to $\alpha\beta$ transformation is necessary and the control has to rely on a correct estimation of the grid phase angle.

2.3.6. Predictive

The predictive control theory was started in 1960's by Kalman [72], and the first patent on a predictive control system for aircraft positioning system was published in 1965 [73]. The application to AC machines control was introduced by Holtz in 1983 [74], minimizing the spatial current vector error in the complex plane. The basic structure of the predictive current control is shown in Fig. 2.15.

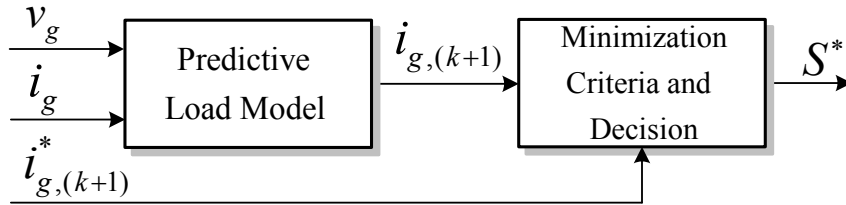


Figure 2.15.: Basic structure of the predictive current control

Based on the load model, the actual and previous measurements, the value of the next sample of the grid current is estimated. Based on the given prediction ($i_{g,(k+1)}$) and the reference current for the next sample ($i_{g,(k+1)}^*$) a switching vector will be selected which must minimize the current error. Next, the selection of the switching vector can be done depending on the predefined minimization criteria which can minimize the switching frequency, minimize the response time or reduce the current distortion.

Based on the described control principle, a new concept for decision on which switching vector sequence will be applied at the next state was introduced in [75]. This method

defines a weighting function which incorporates the minimization criteria. Calculating the weighting function for all the possible vectors that can be applied, the vector with the smallest weighting function is chosen.

The combination of the DPC structure with the predictive selection of the switching vectors sequence was introduced in [76], control structure shown in Fig. 2.16.

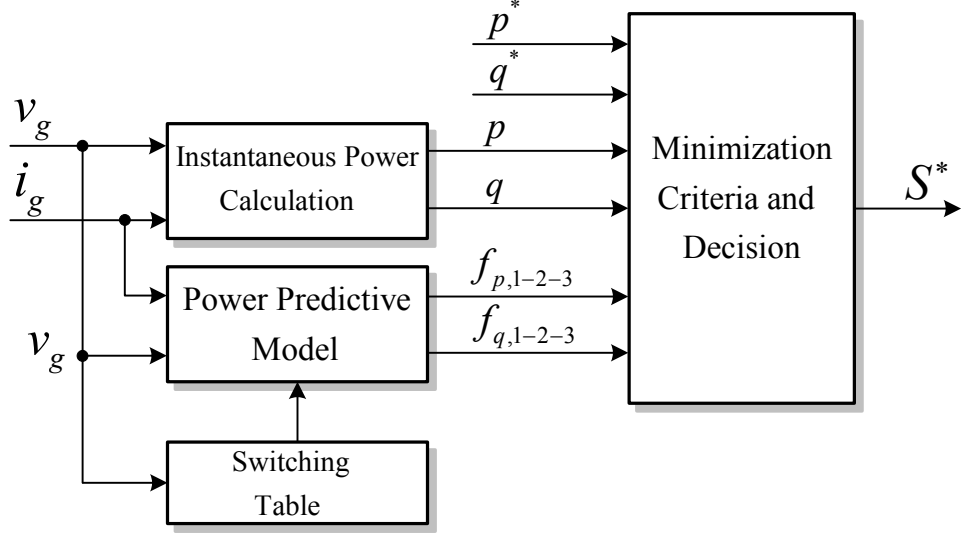


Figure 2.16.: Predictive Direct Power Control

Using the instantaneous power theory the active and reactive powers are calculated. Based on the load model, the active and reactive power slopes ($f_{p,1-2-3}$, $f_{q,1-2-3}$) are estimated for the given switching sequences from the switching table. Having the power slopes and the measured powers at the current sampling, the active and reactive power in for the next sample can be predicted. Therefore, having also the active and reactive power references, based on the imposed minimization criteria the next switching sequence and application time can be computed. One of the selection criteria can be the achievement of constant switching frequency [76].

2.3.7. Passivity based control

Passivity based control (PBC) introduced in 1988 by Ortega [77] is a nonlinear control approach, which uses the energy to describe the state of the system. The system passivity is given by describing the energy flow to/from the ambience, and it was successfully applied in many applications [78, 79, 80, 81, 82]. An energy-based controller shapes the energy of the system in such a way to reach the desired state. The control is achieved by an energy reshaping, injecting damping to modify the dissipation of the system.

The first formulation was based on the Euler-Lagrange equations for energy shaping, mainly suitable for the control of electrical machines [78]. However, for electrical systems,

other formulations were described in the literature: Port-Hamiltonian [83] or Mixed-Potential [84].

Port-Controlled Hamiltonian Systems with Dissipation

The port-controlled Hamiltonian system with dissipation is described by the Eq. 2.1 [85]:

$$\begin{aligned}\frac{dx}{dt} &= [J(x) - R(x)] \cdot \frac{\partial H(x)}{\partial x} + g(x) \cdot u \\ y &= g^T(x) \cdot \frac{\partial H(x)}{\partial x}\end{aligned}\quad (2.1)$$

Here, x is a vector of n dimension, $H(x)$ is the function that represents the total stored energy, $J(x)$ and $g(x)$ are the interconnection matrices, and $R(x)$ is the matrix that represents the dissipation. The interconnection matrices must respect the conditions from Eq. 2.2:

$$\begin{aligned}J(x) &= -J^T(x) \\ R(x) &= R^T(x) \geq 0\end{aligned}\quad (2.2)$$

The energy-balance then is given by Eq. 2.3:

$$\frac{dH(x(t))}{dt} = u^T(t) \cdot y(t) - \frac{\partial^T H(x(t))}{\partial x} \cdot R(x(t)) \cdot \frac{\partial H(x(t))}{\partial x} \leq u^T(t) \cdot y(t) \quad (2.3)$$

Based on the above formulation, two control concepts were defined: Control by Interconnection, and Passivity-Based Control of port-controlled Hamiltonian systems with dissipation [85, 81].

In the *Control by Interconnection*, a desired port-controlled Hamiltonian system with dissipation is imposed in the closed loop, with the matching equation given by Eq. 2.4:

$$[J(x) - R(x)] \cdot \frac{\partial H(x)}{\partial x} + g(x) \cdot u_C(x) = [J_C(x) - R_C(x)] \cdot \frac{\partial H_C(x)}{\partial x} \quad (2.4)$$

Here, the imposed port-controlled Hamiltonian system with dissipation (J_C, R_C, H_C - "controller") must match the plant and the control function is $u_C(x)$ [85, 82]. The controller is given by the state feedback interconnection from Eq. 2.5, where e , e_C are external signals inserted in the feedback.

$$\begin{aligned}u &= -y_C + e \\ u_C &= y + e_C\end{aligned}\quad (2.5)$$

The *Passivity-Based Control* of port-controlled Hamiltonian systems is basically a particular case of the *Control by Interconnection*, where the passivity-based control law is

taken from the state feedback $u = \alpha(x)$:

$$g(x) \cdot \alpha(x) = [J(x) - R(x)] \frac{\partial H_C(G(x) + c)}{\partial x} \quad (2.6)$$

Here the state feedback $u = \alpha(x)$ can be derived from the interconnection of the two systems considered in Eq. 2.4.

Mixed-Potential Function

The Mixed-Potential formulation is based on the following defined function [84]:

$$P(i_L, v_C) = \underbrace{[P_R(i_L) + P_E(i_L)]}_{\text{Current Potential}} - \underbrace{[P_G(v_C) + P_J(v_C)]}_{\text{Voltage Potential}} + \underbrace{[P_T(i_L, v_C)]}_{\text{Circulating Power}} \quad (2.7)$$

Here, the first term is defined as a current potential which is related with the current-controlled resistors and voltage sources, the second term is a voltage potential which is related with voltage-controlled resistors and current sources and the last term is related to the internal circulating power across the dynamic elements (see Eq. 2.8).

$$\begin{aligned} P_R(i_L) &= \int_0^{i_L} v_R(i'_L) \cdot di'_L \\ P_G(v_C) &= \int_0^{v_C} i_G(v'_C) \cdot dv'_C \\ P_T(i_L, v_C) &= i_L^T \cdot \psi \cdot v_C \end{aligned} \quad (2.8)$$

Here, ψ is the interconnection matrix which is determined by Kirchhoff's voltage and current laws.

Based on the Mixed-Potential formulation, the current and DC voltages controls of the cascaded H-bridge converter was developed in [79, 80].

2.4. DC Voltage Control

The grid converter's DC voltage control is activated whenever the supplied/drawn power on the DC side is current controlled. This functionality is also called ACTIVE RECTIFIER OPERATION, and is very common for wind turbines, photovoltaic systems, fuel cells and battery energy storage systems [5]. The general control schematic is shown in Fig. 2.17.

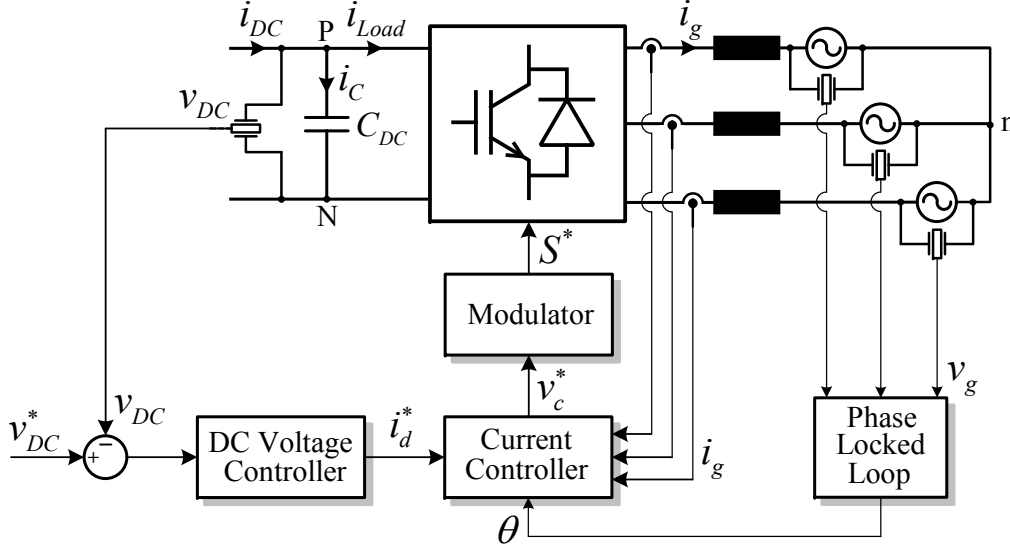


Figure 2.17.: Active rectifier general control structure

The DC-link dynamics is described in Eq. 2.9:

$$C_{DC} \frac{dv_{DC}}{dt} = i_{DC} - i_{Load} - i_C \quad (2.9)$$

Here, i_{DC} is the current supplied/drawn to/from the DC-link capacitor, i_{Load} is the current supplied/drawn to/from the AC grid and i_C is the current supplied/drawn to/from the DC-link capacitor. Thus, the higher the installed capacitance the higher the difference between the supplied and drawn current can be, for a given voltage variation. In complementary, when the load current matches very accurately the supplied current, the installed DC-link capacitance can be reduced to a minimum.

The tuning of the DC control loop is strictly dependent on the installed capacitance. A general approach to chose the minimum DC-link capacitor value, is given in Eq. 2.10 [86]:

$$C_{\min} = \frac{\Delta Q_{C,\max}}{\Delta V_{DC,\max}} = \frac{\max(\int (i_C - i_{C,avg}) dt)}{\Delta V_{DC,\max}} \quad (2.10)$$

Here, $\Delta Q_{C,\max}$ is the maximum capacitor charge variation, which is given by the capacitor current ripple apart from the current drawn by the capacitor itself.

The DC voltage controller from Fig. 2.17 is normally implemented with a PI controller, which is designed using the *symmetrical optimum* principle [87, 4]. The bandwidth of this PI controller must be lower compared with the current controller bandwidth, to ensure decoupling between the two control loops. This leads to slower dynamics in the DC voltage regulation. To improve the DC-link dynamics, feed-forward on the current reference should be used. This can either be implemented by having a measurement of the load current or designing an observer [88].

An important issue in the DC control loop is the situation when there is a second harmonic voltage ripple due to an unbalance in the grid voltage, or when using converter topologies based on H-bridge (see Ch. 6). The usage of an additional resonant controller tuned at the 2nd harmonic frequency was proposed to be used in this situation [89]. However, this solution leads to a distortion of the grid current with a 3rd harmonic. When this situation is not desired, just the feedback filtering of the DC-link voltage should be implemented either by averaging on the 2nd harmonic period or using a notch filter.

2.5. Summary

A brief description of the main control principles used for grid converters was given in this chapter, such as: phase-locked-loop (PLL) methods, linear and some non-linear current control methods and DC-link voltage control.

A review of the PLL methods was given, with implementations for three-phase and single-phase. This is a very important building block in the grid converter control development. Three-phase PLL methods are widely used in three-phase converter due to a simplified implementation and reduced computational burden. Single-phase PLL methods can be used in special cases for three-phase converters when the processing power is available and if the topology requires the independent phase control.

Intensive research on current control strategies over the past years led to the introduction of many different concepts. Linear controllers are widely used in the industry, where the dq frame control is the most spread at the moment. It is disadvantageous that the d and q components need to be decoupled, and this is not ideal. Moreover, the behaviour during unbalanced grid voltage is in question, due to the second harmonic oscillation on the normally DC signals on the d and q axes. Stationary $\alpha\beta$ and natural abc frame controller making use of proportional resonant regulators are an alternative, to overcome this unpleasant situation. In the $\alpha\beta$ control, the axes are naturally decoupled, and both the positive and negative sequences are controlled at the same time with the same controllers. However, the generation of reference signals is very important, and must be carefully implemented. Hysteresis and direct power control techniques are interesting alternatives, which are very robust and with excellent dynamic performance. However, implementations with constant switching frequency and well defined current spectrum must be considered. Predictive control is an emerging technique, where the minimizing criteria can bring important benefits for different applications. However, its dependency on the load parameters and high computational burden are the main disadvantages. Passivity based control is a nonlinear control concept, that uses the energy to describe the state of the system. It was shown that using control structures based on this concept gives robustness against load parameter variation and enhances the overall operation stability.

When operating the grid converter in active rectifier mode, which is in most of the cases, the second harmonic ripple on the DC-link must be taken into consideration when designing the control loop. Moreover, with the trend to reduce the installed capacity and therefore reduce the decoupling between the supply and load, the proper DC voltage control must be ensured.

Chapter 3.

Active Rectifier Implementation for a HV Energy Storage Test Bench

This chapter presents the design, control and experimental results of a LV two-level active rectifier, grid connected through an LCL filter, implemented for a HV battery energy storage test bench

3.1. Introduction to the Energy Storage Test Bench

The increase of power generation based on volatile sources as wind and solar requires special considerations for power management in electrical networks. The power management can be done using conventional power plants or energy storage systems. Conventional power plants are more efficient having a stationary or predictive load situation. Energy storage is the key technology to integrate renewable energy sources on large scale into the present power systems, without compromising its stability. Storage systems can partially compensate the fluctuations of the volatile power sources. Battery energy storage systems offer scalable solutions for high power and high energy demands of up to 100 MW and 100 MWh [90, 91]. When the installed power goes up to the highest levels, series connected batteries will be necessary to reduce the current levels and thus the overall system losses. The charging and discharging characteristics of series connected batteries up to several kV is unknown. To test the operating behaviour of 360 series connected 12 V lead-acid battery blocks, a test bench with 100 kW and 120 kWh was realized [92].

The test bench power electronic interface has a two stage conversion, consisting of a galvanic insulated 3-level/2-level dual-active bridge DC-DC converter and a 2-level DC-AC converter, for the 50 Hz, 400 V_{LL} grid connection, see Fig. 3.1. The DC-DC converter has a maximum transformation ratio of 8 and acts as a charging/discharging unit, controlling the batteries' current. The power rating transfer is between 5 kW and 100 kW.

To fix the DC-DC converter's transformer potential on the high voltage side, the 3-level's neutral point and the battery stack midpoint are connected and grounded. On the low

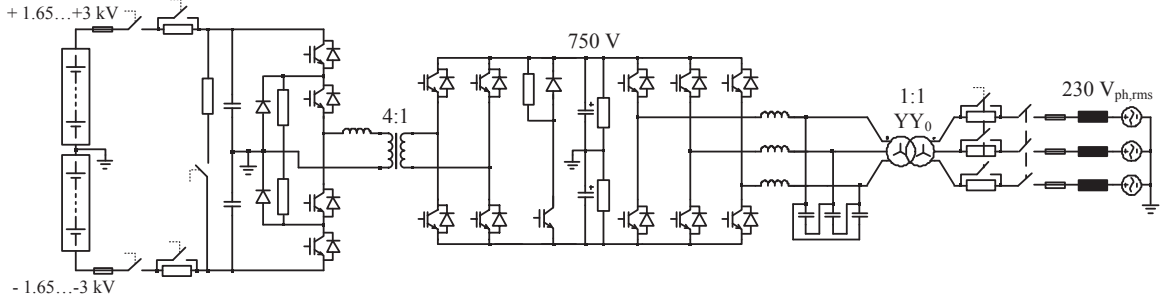


Figure 3.1.: Test bench power electronic interface

voltage side, the DC-link midpoint is grounded. This will indirectly fix the potentials of both transformers. This is also the path for the inherent common mode currents of both low voltage converters.

The installed DC-link capacitance between the DC-DC converter and the inverter is a trade-off between the capacitors price and maximum allowable voltage ripple. The DC-DC converter is switched with 1 kHz, producing a current ripple which is absorbed by the common low voltage DC-link. The DC-AC converter is switched with 3.15 kHz and controls the grid current with a power factor of ± 1 , with a DC voltage control as outer loop. Therefore, the dimensioning must take into account the achievable DC control bandwidth to keep the ripple at a level where the current loop is not affected.

3.2. Hardware breadboard of the DC-AC converter

The grid side converter uses the classical 2-level hard-switched topology with a LC filter having delta connected capacitors and a low frequency transformer for insulation, see Fig. 3.2. The transformer acts also as filter inductor on the grid side, considering its leakage inductance. The Yy_0 winding connections allow the propagation of asymmetrical grid faults in all three phases in the transformer winding on the converter side [93]. This is an important advantage for the current control loop stability.

Inrush current limiting resistors are installed to reduce the DC-link capacitors charging current, the free-wheeling diodes current and the transformer magnetizing current. The grid converter's rated power is 110 kVA. Thus, it theoretically can provide or consume reactive power on demand while charging/discharging the batteries at rated current (145 A_{rms}). The chosen filter inductance is $L_f = 0.2$ mH at rated power and filter capacitor of $C_f = 47$ μ F, resulting in an attenuation of around 30 dB at the switching frequency of 3.15 kHz. The filter capacitors' and inductors' parasitic resistances are in the range of m Ω and thus a small natural filter damping is achieved.

Measurement of the grid current for the inner control loop is done on the grid side of the equivalent LCL filter, using hall sensors for each phase to avoid the cumulative error when

3.2. Hardware breadboard of the DC-AC converter

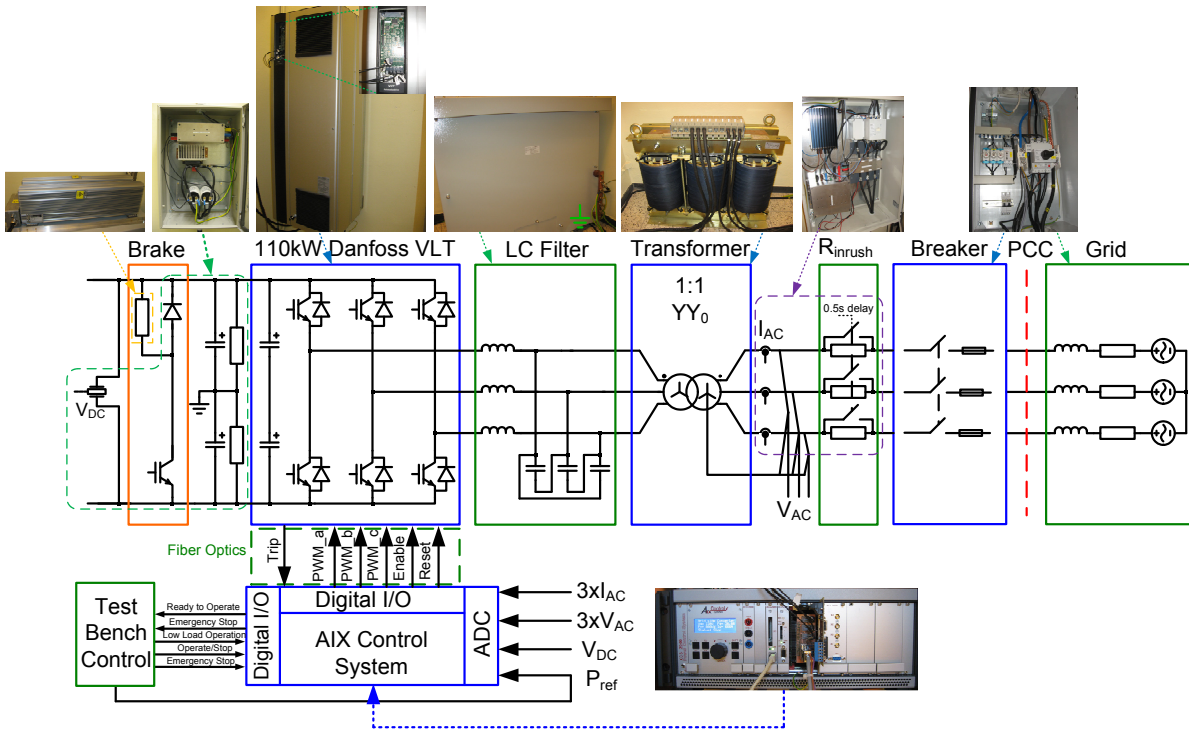


Figure 3.2.: Grid converter test setup

using two sensors only. This solution has the advantage of achieving stable operation without damping, and natural achievement of the unity power factor¹ operation of the current control when the reactive current reference is set to zero [94]. The grid voltages are sensed on each phase at the coupling point.

The output power of the DC-DC converter can be controlled much faster than the output power of the DC-AC converter. The DC-DC converter is capable of switching between positive full power to negative full power during one switching period. Thus, in case of a grid disconnection/fault while discharging batteries there is the possibility of common DC-link overvoltage, in the worst case scenario when the DC-DC converter does not reduce the transfer power. Therefore, as an additional hardware protection, a brake chopper was installed in the DC-link with trigger from an independent control platform as a last layer of the protection system.

¹Power factor is with respect to the coupling point. The power factor with respect to converter is always capacitive, to provide the necessary reactive power consumed by the filter inductors and output transformer.

3.3. Control of the DC-AC grid converter

The test bench control sets the reference power, flowing to or from the batteries depending on the operation mode, state of charge and voltage balancing. The batteries' voltage is changing very slowly with the state of charge. Therefore the DC-DC converter control calculates the reference DC current from the reference power. Thus, the batteries' current is the only control parameter of the DC-DC converter and this is the only unit which controls the transferred power. Its bandwidth would allow the control of the common DC-link voltage, but this is not intended because the purpose is to directly control the batteries' current. The overall test bench control can therefore set the constant power or constant current charge/discharge modes. The common DC-link voltage is controlled by the grid converter to be constantly 750 V. The voltage level assures a sufficient control margin to inject/draw full power for a wide grid impedance variation. Ideally, to optimize both converters' losses, the level should be adjusted depending on the required power transfer and grid impedance. Having both converters controlled by separate platforms and for control simplicity the common DC-link voltage is kept constant. The DC-link voltage error dictates the DC-AC converter's active power transfer, while the test bench power reference is taken as feed-forward to help the voltage controller during transients.

The grid converter control structure regulates the DC-link voltage to achieve the power balance between the two interconnected sources, regulation achieved by controlling the grid current as inner loop synchronized with the grid voltage. A proportional integral (PI) controller is normally employed for DC voltage regulation, which acts on the active current exchange with the grid while the active power reference given by the test bench control improves the controller transient response, see Fig. 3.3.

The reactive current can be controlled with the feed-forward term. However, there is no need to inject reactive power for this test bench and only active power transfer is realized. For the current control there are several possibilities with respect to the chosen reference frame in the case of linear controllers, hysteresis control or predictive control [57]. The stationary frame control ($\alpha\beta$) was used in this work since it provides the following advantages: fixed defined current spectrum, low dependency on grid impedance variation, no cross coupling terms required, grid voltage feed forward is not required and the harmonic compensation (HC) can be easily implemented in the same control frame for the low frequency components. The influence of the grid voltage harmonics on the current controller can be reduced with this structure. Using the resonant integrators, the injected grid current harmonics which are by nature present in the current feedback are compensated.

A phase-locked-loop (PLL) structure that is able to filter the grid voltage from harmonics and extract the positive sequence for synchronization was used [34], see Fig. 3.4. The double second order generalized integrator (DSOGI) filters the $\alpha\beta$ components and the positive-negative sequence calculator (PNSC) is used to extract only positive sequences

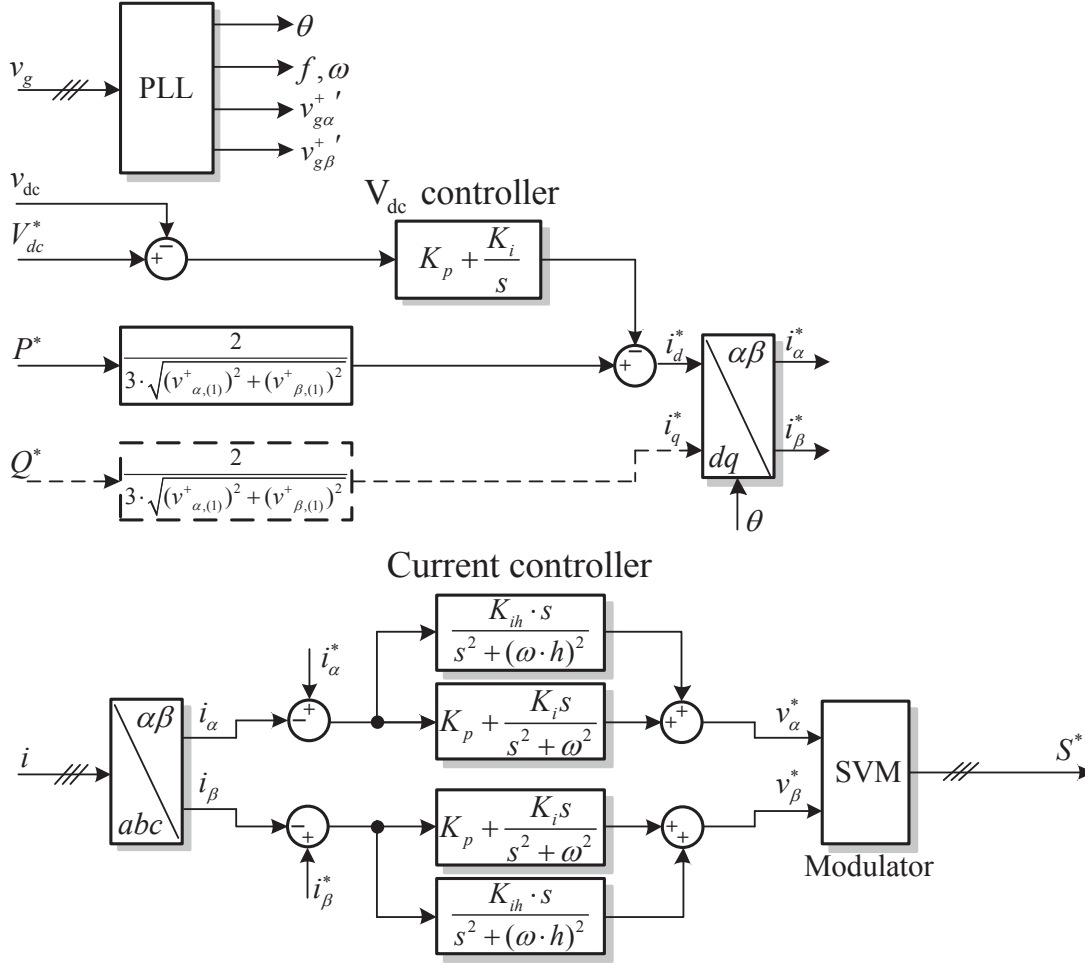


Figure 3.3.: Grid converter control structure

for synchronizing in the synchronous reference frame PLL (SRF-PLL). It was shown that this structure provides very good accuracy with relatively small computational cost.

Discretisation of the SOGI, as well as for the resonant integrators used in $\alpha\beta$ current control was realized using the Euler method, as shown in [35]

Depending on the batteries state of charge and the requested converter functionality, the control can be further enhanced with partial or total voltage harmonic compensation for the required frequencies.

Having the current sensed on the grid side, neglecting the parasitic resistances of inductors and capacitors, the following transfer function characterizes the plant [94]:

$$G_{LCL}(s) = \frac{i_g(s)}{v_c(s)} = \frac{1}{L_g L_f C_f s} \frac{1}{(s^2 + \omega_{res}^2)}, \text{ where } \omega_{res} = \sqrt{\frac{L_f + L_g}{L_g L_f C_f}} \quad (3.1)$$

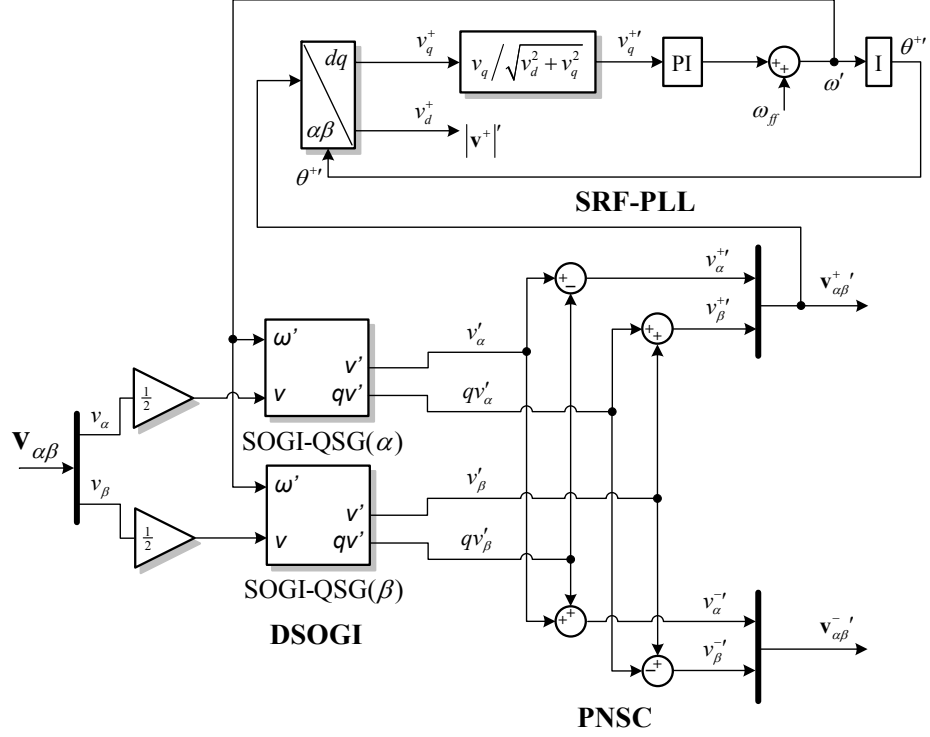


Figure 3.4.: Double SOGI Phase-Locked-Loop algorithm [34]

Here, L_g represents the total inductance on the grid side (grid and transformer leakage inductances). The point of common coupling parameters were measured, characterized by an impedance in the range of $0.2 \, \Omega$ to $0.3 \, \Omega$ mostly resistive, translated in a short circuit current around 1 kA. To ensure a stable filter grid connection, the harmonics at its resonant frequency (1.34 kHz) need to be avoided. The grid voltages spectrum is shown in Fig. 3.5. It can be noticed the high magnitude of the 7th harmonic which is reflected in the current spectrum without compensation, as shown in the experimental results (see Fig. 3.10).

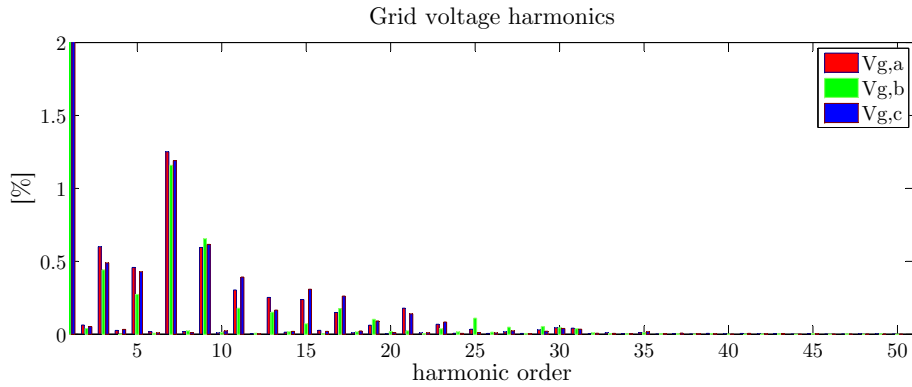


Figure 3.5.: Grid voltage harmonics at the coupling point

Typical control implementations are performed with sampling frequency equal with the switching frequency where the point of data acquisition is at maximum or minimum of the triangular carrier. In this case (single edge sampling) the equivalent closed loop control delay is $1.5 T_{SW}$ (switching periods). In this work, to reduce the closed loop delay further, the sampling takes place at both maximum and minimum of the triangular carrier (double edge sampling) as seen in Fig. 3.6. This results in an equivalent closed loop delay equal with T_{SW} [95].

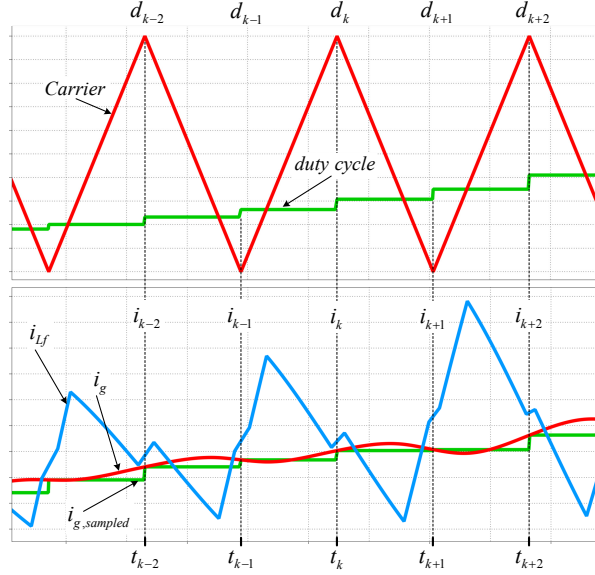


Figure 3.6.: Measurements double edge sampling

As seen in bode diagram from Fig. 3.7, the magnitude peak at filter's resonant frequency is reduced due to the filter capacitor's parasitic resistance.

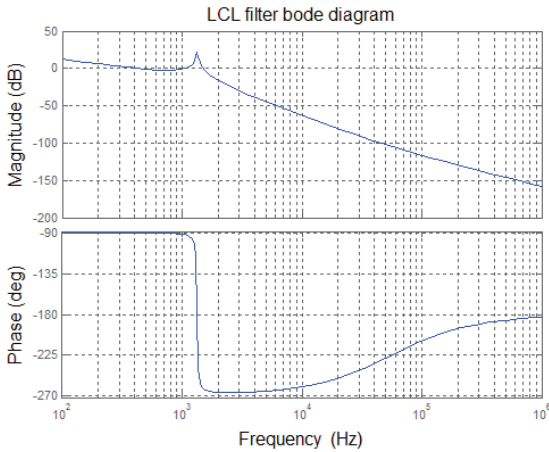
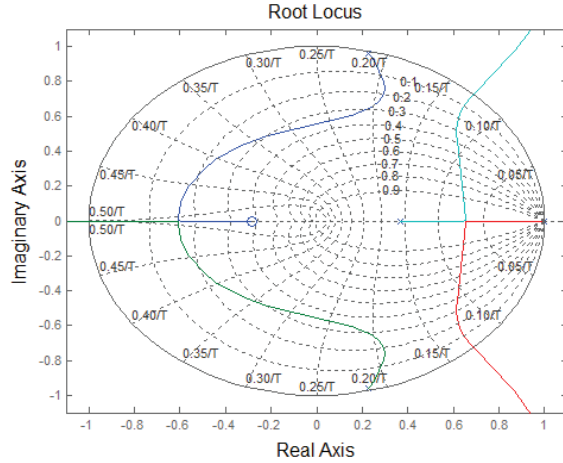


Figure 3.7.: LCL filter bode diagram


 Figure 3.8.: Root locus with $f_s = 2f_{sw}$

Stability margin can be achieved without damping, with the gain range given in the root locus from Fig. 3.8 using double sampling frequency ($f_s = 2 \cdot f_{sw}$).

3.4. Active rectifier interaction with DC-DC converter

To meet the stability requirement under transient conditions, the control bandwidths of the slowest loop sets limitations of the other control parameters. In the present case, the DC-AC converter control bandwidths are limited by the switching frequency and the filter resonant frequency. The inner control loop must be tuned to operate below the filter resonant frequency and to fit the LCL stability margin. The DC-link voltage control as outer loop must be tuned with more than twice smaller bandwidth to ensure the stability margin. The DC-link capacitor's voltage variation is given by Eq. 3.2. During transients, the DC-DC converter's dP/dt is limited by Eq. 3.3 for a given maximum voltage variation.

$$v_C(t) = \frac{1}{C} \int_{t_0}^t i_C(t) \cdot dt + v(t_0) \quad (3.2)$$

$$\frac{dP_{\max,DC-DC}(t)}{dt} = V_{DC,DC-AC}^* \cdot \frac{di_{C,\max}(t)}{dt} = V_{DC,DC-AC}^* \cdot C \cdot \frac{d^2V_{DC,\max}(t)}{dt^2} \quad (3.3)$$

The DC-link capacitor's current during transient and steady state is given by:

$$i_C(t) = i_{DC-DC}(t) + i_{d,DC-AC}(t) \quad (3.4)$$

Here the DC-DC converter current is the low voltage DC-link current which is indirectly controlled with respect to the battery's controlled current. The d axis current is imposed by the grid converter's DC-link voltage control. For the present application the theoretical maximum dP/dt was set to 1 kW/ms for a maximum dV_{DC}/dt of 2 V/ms (40V/20ms) with an installed DC-link capacitance of 13.6 mF.

Regarding the DC-link capacitors' size, the maximum allowable ripple current must be considered. A simulation model of both converters was performed. The converters interaction during discharge steady state mode at 100 kW is presented in Fig. 3.9.

Due to unsynchronized switching states between the DC-AC and the DC-DC converters, an increased capacitor's current ripple can be noticed. The DC-DC current harmonics are centred at twice its switching frequency and multiples due to the low voltage H-bridge, while the DC-AC converter's DC current harmonics are centred at twice the switching frequency. Thus, according to Eq. 3.4, the ripple currents of both converters are found on the capacitor's current. This current ripple can be reduced by choosing

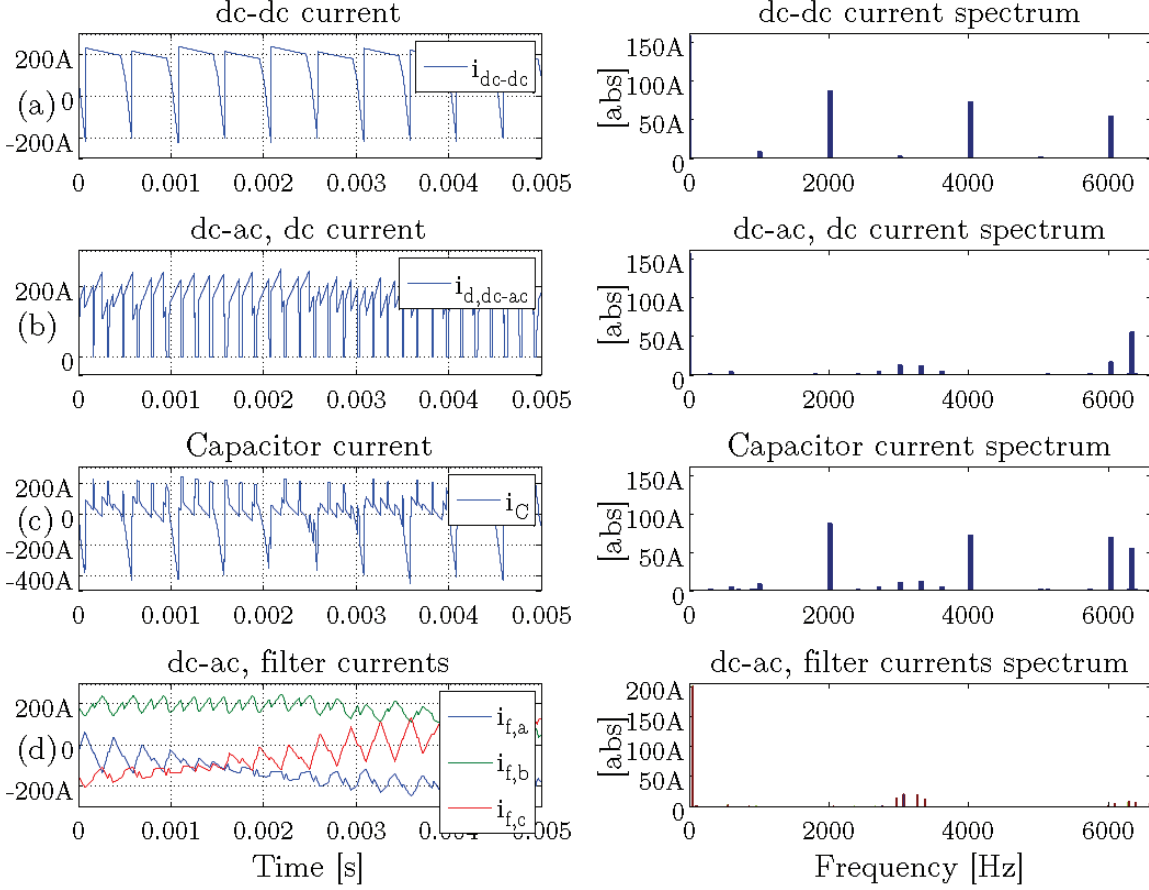


Figure 3.9.: Interaction of the DC-DC and DC-AC converters for discharge operation

the DC-AC converter's switching frequency as exact multiples of the DC-DC converter switching frequency, together with a modulation carrier's synchronization. Further ripple reduction can be achieved using a three-phase DC-DC converter [96].

3.5. Experimental results

Each converter is controlled with its own control platform. In the first stage, the grid converter was tested as stand-alone using a power supply to emulate the DC-DC converter and the series connected batteries.

Fig. 3.10 shows the current controller operation without harmonic compensation (only the fundamental resonant compensators). Here the power supply is voltage controlled and the DC-AC grid converter's voltage control loop is not enabled. As expected from the grid voltage harmonic analysis (see Fig. 3.5), distortion of the grid current is with high magnitude of the 7th harmonic. Implemented current control parameters are $k_p = 2$ and

$k_i = 1000$ selected to achieve a bandwidth of around 500 Hz. In Fig. 3.11 the harmonic compensation for 7th harmonic was enabled with the integrator gain $k_{ih} = 500$, and the current at this frequency was brought to zero.

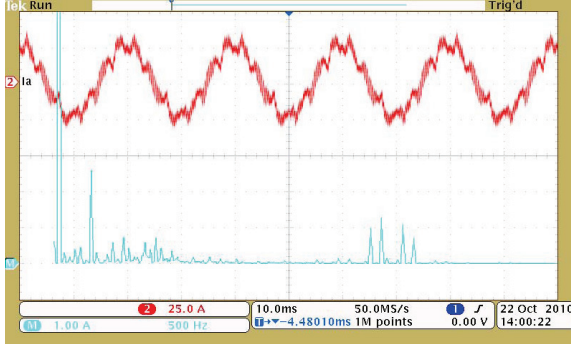


Figure 3.10.: Current control without HC

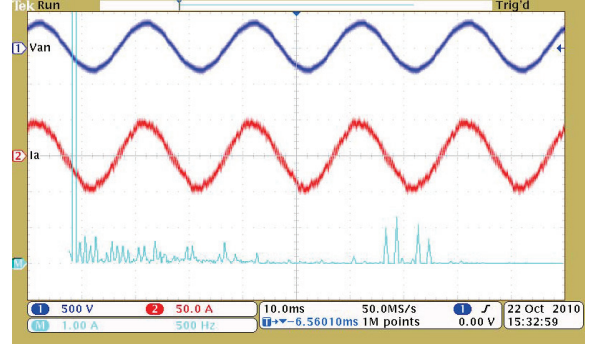


Figure 3.11.: Current control with HC

In Fig. 3.12.(a,b,c,d) the experimental results are shown for light load operation, limited by the power supply ratings. Data was recorded from the control platform and plotted. Here the power supply is current controlled and the grid current is positive (emulated discharge).

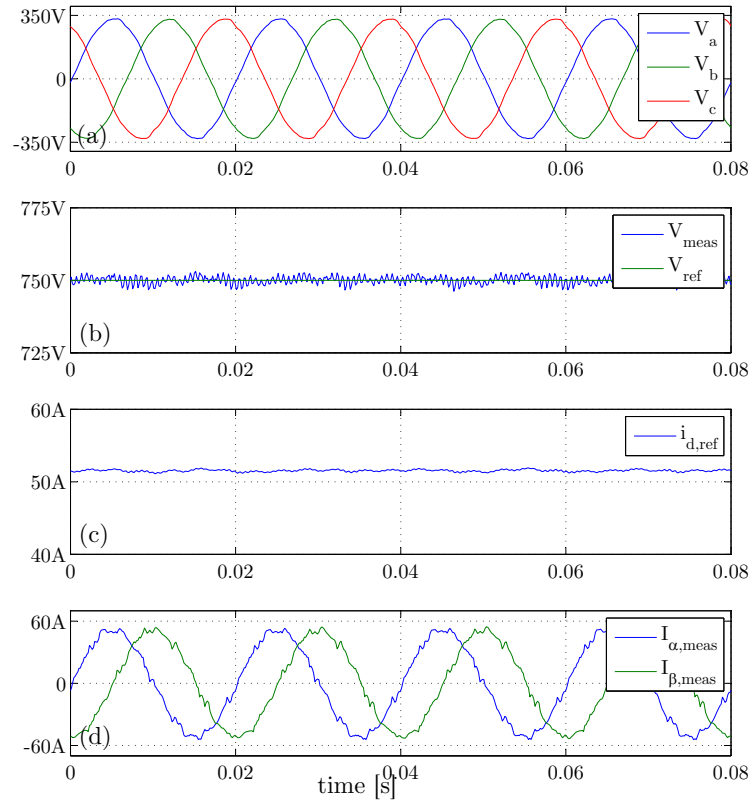
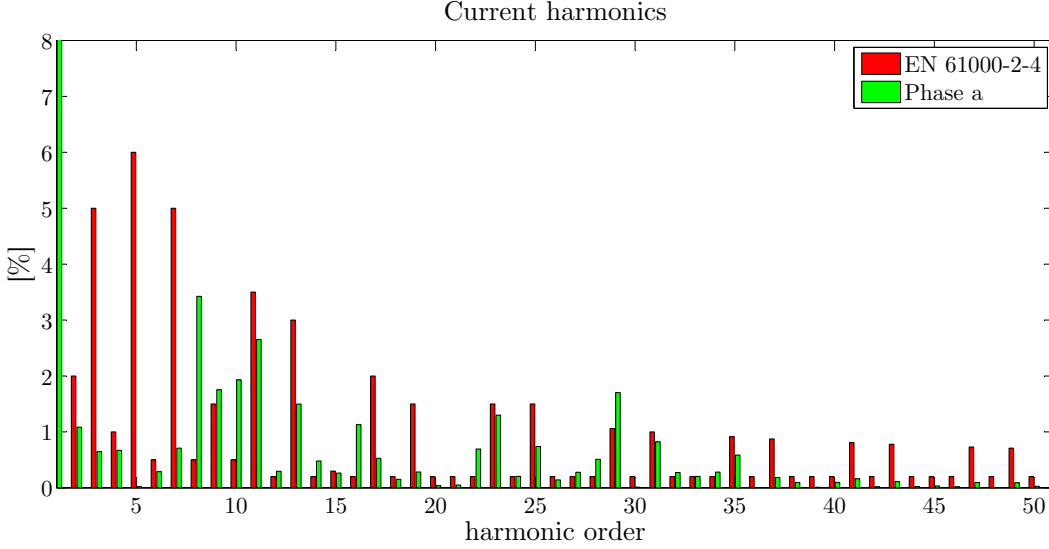


Figure 3.12.: Active rectifier light load experimental results

The phase *a* current spectrum against the harmonic standard EN 61000-2-4 is shown in Fig. 3.13, for the light load operation mode from Fig. 3.12. The current control uses harmonic compensation for 5th and 7th harmonics and the voltage control parameters are $k_p = 0.2$ and $k_i = 10$. It can be noticed the low magnitude of odd harmonics, even at light load (20 kW). It is interesting to notice the increase of 8th and 10th harmonics at this operation mode. The 10th harmonic is equivalent to 500 Hz for the 50 Hz grid, and this is the frequency around the current controller bandwidth.

Figure 3.13.: Phase *a* current spectrum

3.5.1. Experimental results in the Test Bench

The measurements during operation of both converters (DC-DC and DC-AC) with bidirectional power transfer between grid and the high voltage battery are presented in Fig. 3.14. Firstly, the DC-AC converter is turned ON (at 19 s on time scale) and controls the DC-link voltage to 750 V with no load. The DC-DC converter is turned ON next (at 46 s), charging the batteries with 20 kW and the power flow is reversed at 250 s from -20 kW to +50 kW, discharging the batteries. It can be noticed that the DC-AC converter controls the DC-link voltage smoothly over the entire operation.

The difference of the measured DC-link voltage during batteries charge procedure, compared with the discharge procedure when the voltage is fixed at exactly 750 V is given by the integration method used for the DC control loop PI controller. The implemented integration method was done with the Forward Euler method, and this explains the steady state error when the PI input error is positive. The usage of the Forward and Backward Euler methods for the discharge and respectively charge modes, or the Trapezoidal method for both operation modes will remove the steady state error.

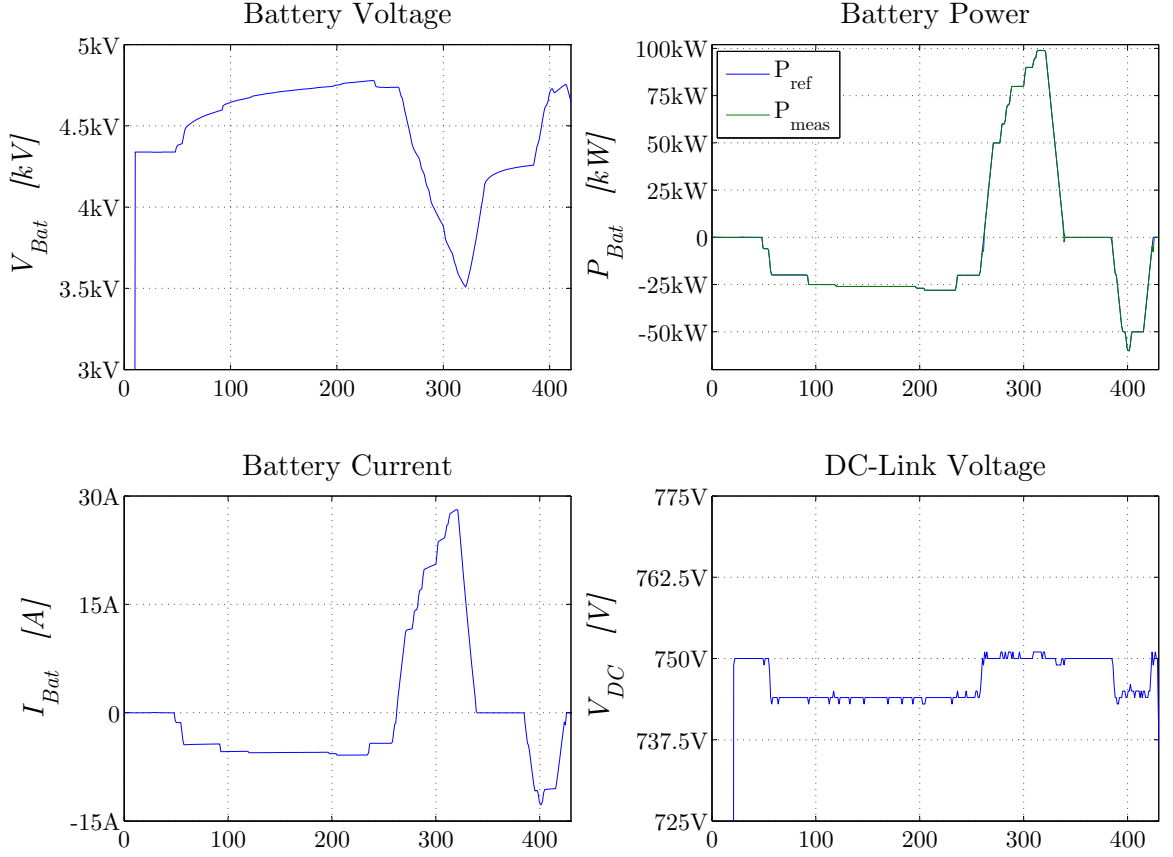


Figure 3.14.: Full power test bench experimental operation

The DC-DC converter dP/dt limit during experiments was set to 0.3 kW/ms for smooth transients. The battery series connection consists of lead-acid battery blocks. Therefore, when discharging at full power, the battery voltage drops significantly from 4.7 kV to 3.5 kV. This is due to their impedance and delivery of stored energy.

3.6. Summary

The design, control and experiment of a LV DC-AC grid converter was presented in this chapter. The implementation was realized for a 6 kV battery energy storage test bench, with a rated power of 100 kW. The power electronic interface is a two stage topology, consisting of a two-level DC-AC grid converter and a two-level/three-level dual active bridge DC-DC converter. The DC-DC converter controls the battery current of the high number of series-connected batteries. The DC-AC grid converter is in charge of controlling the common DC-link voltage and the grid currents.

The grid connection was realized via a LC filter and transformer which is equivalent to an LCL filter. The stationary frame $\alpha\beta$ current control was implemented, and the system

was proved to be stable without damping. The harmonic compensation is critical to be used, because of the background distortion present in the grid voltages. Increased harmonic distortion of the grid current, at light load, was seen around the frequency where the current control bandwidth is tuned. However, at rated power operation it is expected that the system will be more damped and this harmonics will be reduced below the limits of the grid connection harmonic standard.

The complete test bench functionality with bidirectional power flow of up to 100 kW was verified and presented.

Part II.

Medium Voltage Grid Converters for
Energy Storage

Chapter 4.

State-of-the-Art on Medium Voltage Multilevel Converters

This chapter presents the survey on multilevel converters suitable for medium voltage, with a view from the perspective of usage in stationary battery energy storage

4.1. Introduction

Multilevel converters represent the improved way of classical two-level converters to convert energy, with the basic concept developed in the early 1960's [97]. The basic idea is to synthesize a sinusoidal voltage in several voltage steps. The voltage steps can be achieved from series connected capacitors or isolated voltage sources. Many advantages of multilevel converters have been reported, as: smaller semiconductor voltage ratings, the improved output voltage quality, low electromagnetic compatibility concerns. In medium and high voltage conversion, the multilevel converters are a necessity.

Multilevel voltage source converters can be found in different configurations. In principle, the building cells for multilevel converters are: two-level half bridge, two-level H-bridge, neutral point clamped and flying capacitor derived from two-level converter using series connected switches with clamping elements. Going forward with these cells, combinations between them give birth to new converters in a large variety [98].

4.2. Cascaded H-bridge Converter

Cascaded H-Bridge (CHB) Voltage Source Converter (VSC), developed in 1970's [99, 100], was the first approach for multilevel conversion. Firstly it was controlled to achieve a staircase waveform to approximate the sinusoidal voltage, and later on Pulse Width Modulation (PWM) and Space Vector Modulation (SVM) were applied [101]. To minimize the switching losses, the selective harmonic elimination technique (SHE-PWM) can

be applied [102, 103]. From its early development, the CHB converter was designed as battery charger/discharger to store energy from other generation units with higher voltages [100]. The application to a transformerless system with grid coupling at 6.6 kV is given in [104], making use of supercapacitors in each converter cell DC-link to eliminate the disadvantage of second harmonic current drawn from batteries. The three-phase five-level CHB converter is shown in Fig. 4.1.

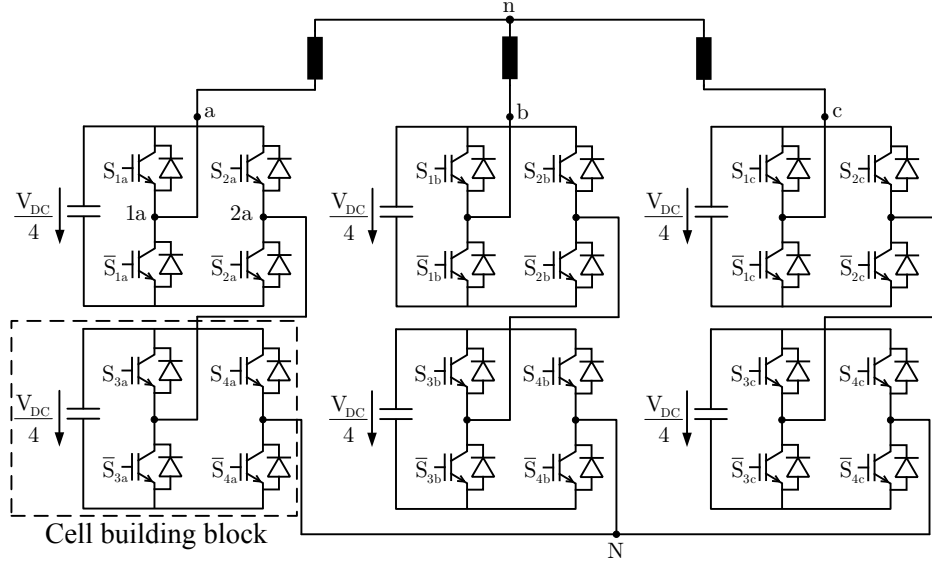


Figure 4.1.: Five-level Cascaded H-bridge VSC [100]

This topology can be classified as hard or soft switched, as well as with symmetric or asymmetric DC power supplies. The converter construction is based on the classical two-level full bridge converters which are connected in cascaded to increase the output voltage and output levels. The number of output levels is proportional with the number of cascaded cells. For the symmetrical construction, the isolated DC sources have the same values for all H-bridges. Increasing the number of levels (more converter cells) the converter output redundancy for the intermediary voltage levels (below the peak voltage) are increased direct proportional. These degrees of freedom can be used to achieve a better harmonic spectrum or the switching frequency can be reduced, depending of the application where the converter is used.

The symmetrical CHB converter (Fig. 4.1) has the following advantages and disadvantages:

Advantages:

- + modular solution
 - design flexibility
 - increased availability → if an additional redundant cell is installed
- + high efficiency conversion due to direct coupling to grid
- + low switching frequency operation
 - low switching losses
- + construction with well proved components from industry → low voltage batteries and power electronics
- + small output filter due to high output redundancy and output voltage levels

Disadvantages:

- high number of devices
 - increased number of gate drivers
 - increased overall failures in time (FIT) rate
- second harmonic on batteries current
 - high DC-link capacity required
- high conduction losses (proportional with the number of cells)
- high leakage current due to battery cells voltage and coupling to ground
 - considerations on capacitive coupling reduction

Another family of CHB converters is the CHB with unequal DC sources [105, 101]. This converter class is an alternative to symmetrical CHB which reduce the number of DC sources for a certain given output levels. Basically, the idea is to have an H-bridge cell which is powered with two or three times bigger voltage than the other one, like in Fig. 4.2.

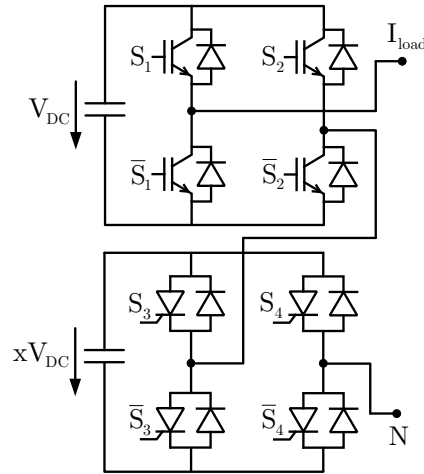


Figure 4.2.: Seven or Nine-level Asymmetric CHB VSC [105]

Because the second cell voltage rating is higher, Integrated Gate Commutated Thyristors (IGCT) can be used with reduced switching frequency, and Insulated Gate Bipolar

Transistors (IGBT) in first cell switching at high switching frequency, converter being classified as hybrid. The modulation of hybrid CHB is achieved using combined PWM with staircase modulation; the high voltage cell (or cells) is switched at fundamental frequency and the low voltage cell is switched at high frequency. Using the Asymmetric CHB (ACHB) the output voltage levels are maximized, creating voltage levels also in power supply, and in the same time the converter output redundancy is eliminated. However, the converter modularity is affected because unsymmetrical construction will be adopted.

The ACHB converter (Fig. 4.2) has the following advantages and disadvantages in addition to the symmetrical CHB:

Advantages:

- + higher efficiency
 - usage of combined devices technology (slow and fast switches)
- + output levels maximization

Disadvantages:

- partial modularity
- increased control complexity
 - voltage balancing
 - batteries SOC balancing
- no fault management

In order to nearly eliminate the switching losses of the devices, resonant circuits can be applied for multilevel converters. Therefore the operating switching frequency can be increased, the result being a reduction of the output filter. Many resonant solutions were presented, for instance the Auxiliary Resonant Commutated Pole [106] (ARCP) will be considered to be applied to H-bridge converter. The resulting configuration is depicted in Fig. 4.3.

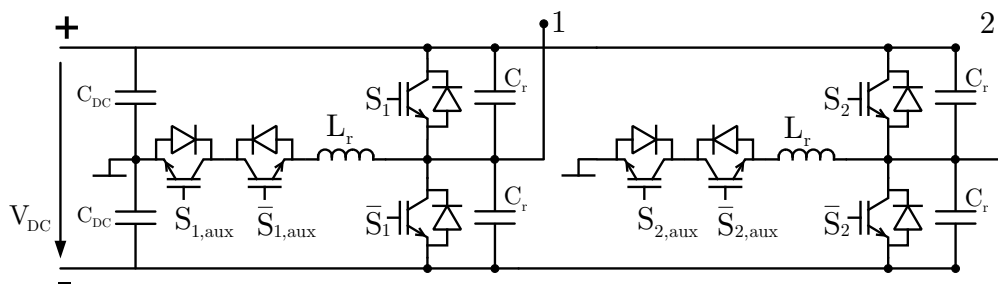


Figure 4.3.: ARCP H-bridge converter cell [106]

In addition to the basic H-bridge configuration, the cell DC-link is split in two series connected capacitors and has the following auxiliary devices: four resonant capacitors C_r , two resonant inductors L_r and four auxiliary switches S_{aux} . The auxiliary switches are operating under zero-current switching, while the main switches operate under zero-voltage switching. Thus the auxiliary switches can be dimensioned for lower current ratings. However, auxiliary switches experience high peak currents and therefore their

dimensioning is not optimal. In order to decrease the turn OFF losses, the size of the resonant capacitors can be increased.

An important advantage of the ARCP over the other resonant circuits is the possibility to apply PWM. It has the ability to stop and release the resonance at precise moments. However, a more complicated control strategy must be adopted to keep the resonance with the help of auxiliary switches. Furthermore, even if full soft-switching is achieved, the turn OFF losses are not eliminated completely due to the IGBT tail current and a part of the saved losses will be moved in the auxiliary circuit.

The soft-switched cascaded H-bridge converter (cell structure in Fig. 4.3) has the following advantages and disadvantages in addition to the symmetrical hard-switched CHB:

Advantages:	Disadvantages:
+ reduced switching losses	- poor auxiliary switches utilization
→ possibility to increase efficiency	→ high peak currents
→ reduced ratings for the main switches	- losses in the auxiliary circuit
+ increased switching frequency operation becomes feasible	- increased number of components
→ output filter reduction	→ higher overall FIT rate
→ decreased number of cells	→ increased converter size
	- increased control complexity

4.3. Neutral Point Clamped Converter

The Neutral Point Clamped (NPC) VSC was the second developed multilevel converter, patented in 1980 [107] and firstly introduced in [108]. The three-level converter configuration is shown in Fig. 4.4, topology applied for active and reactive power compensation in [109].

For even number of levels the midpoint is not accessible. Increasing the number of levels above three, the capacitors voltage balancing becomes an important problem. Furthermore, when the number of levels is increased the conduction losses become more important and the utilization of the clamped diodes becomes poor. A control strategy that achieves the voltage balancing at high modulation indexes was developed in [110], improvement paid with an increased number of commutations.

An important drawback is the unequal loss distribution among the semiconductors, issue which was studied in [111], and the Active Neutral Point Clamped converter was introduced. It was shown that the outer switches (S_1 and $\overline{S_2}$) are more stressed in

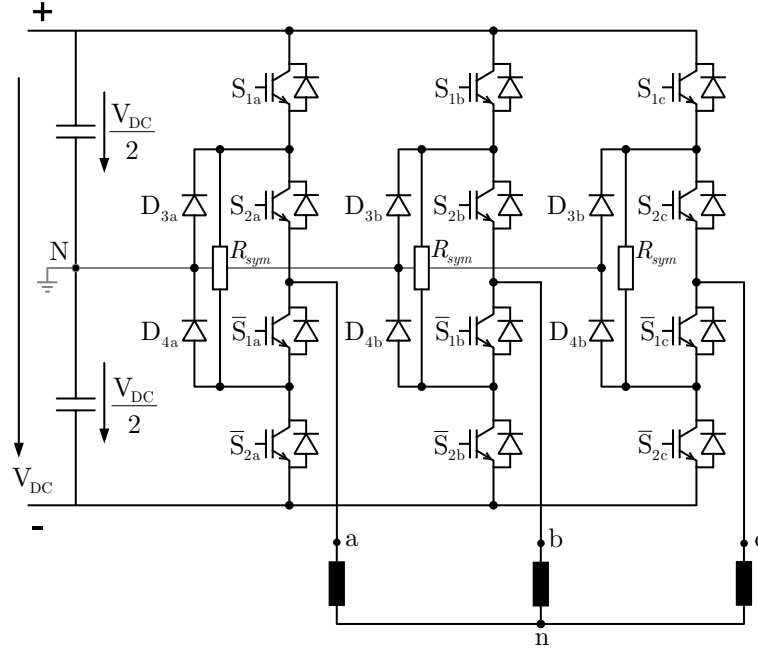


Figure 4.4.: Three-level Neutral Point Clamped VSC [108]

comparison with the inner switches (S_2 and \bar{S}_1) at high modulation indexes and ± 1 power factor (PF).

The modulation strategies applied to this topology are level-shift PWM (LS-PWM), which can be applied with different carrier disposals. As the NPC switching states are just three (no redundancy), three-level SVM is well applied also. Nevertheless, various discontinuous PWM techniques (DPWM) are available and could be implemented as well with similar performances [101].

The NPC converter (Fig. 4.4) has the following advantages and disadvantages:

Advantages:

- + low cost solution
- + high efficiency
- + control simplicity

Disadvantages:

- unequal loss distribution in devices
- not suitable for higher number of levels than three
- no modularity
- unequalized device voltage stress \rightarrow symmetry resistors are necessary

Soft switching technology is applied to NPC converter too. Several converters were proposed for soft-switch three-level conversion [112, 113]. A topology which reduces the auxiliary elements, using one resonant circuit for all the converter phases, is presented in

[113]. Due to reduced number of the auxiliary passive components and the possibility of PWM operation capability, the ARCP NPC converter shown in Fig. 4.5 it is a promising solution for high power applications [114]. In addition to the NPC converter, the DC-link is divided in four, three resonant capacitors one inductor and four bidirectional switches are used to achieve zero-voltage switch to its main switches. Since the switching losses are reduced the PWM switching frequency can be increased. Therefore the increased converter price by the auxiliary components can be compensated by a reduction of the output filter size and the reduction of main switches silicon area. However, special attention must be paid in the design of the resonant passive components which can become important source for losses.

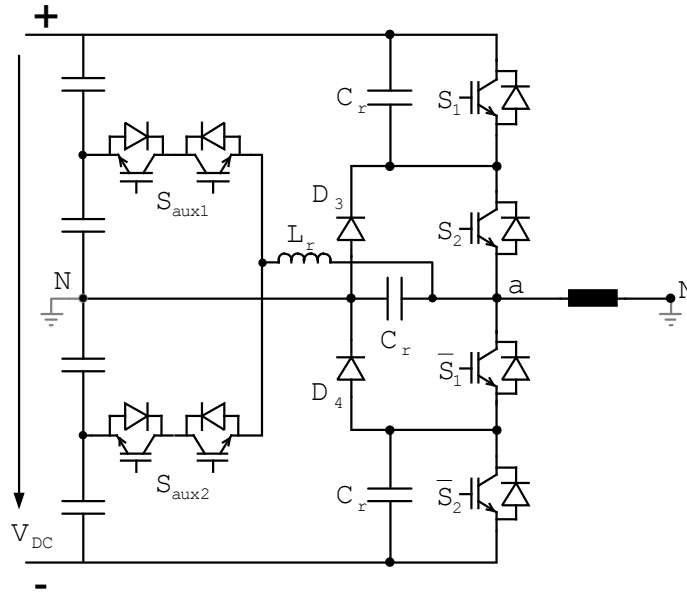


Figure 4.5.: Three-level ARCP NPC VSC phase leg [114]

The soft-switched NPC converter (Fig. 4.5) has the following advantages and disadvantages compared with the hard-switched NPC:

Advantages:

- + reduced switching losses
 - possibility to increase efficiency
 - reduced ratings for the main switches
- + increased switching frequency operation becomes feasible
 - output filter reduction

Disadvantages:

- poor auxiliary switches utilization
 - high peak currents
- losses in the auxiliary circuit
- increased number of components
 - higher overall FIT rate
 - increased converter size
 - increased price
- increased control complexity

4.4. H-bridge Neutral Point Clamped Converter

The H-bridge Neutral Point Clamped (HNPC) [115, 116] is a hybrid converter topology between the CHB and the NPC converters. Instead of using two-level half-bridges as a building block for the H-Bridge, in this structure the three-level half-bridge is used. The resulting five-level converter topology supplied from isolated DC power sources is shown in Fig. 4.6. The application using only one high power DC source will require the grid connection via an open winding transformer, similar solution applied in Alaska by ABB [117].

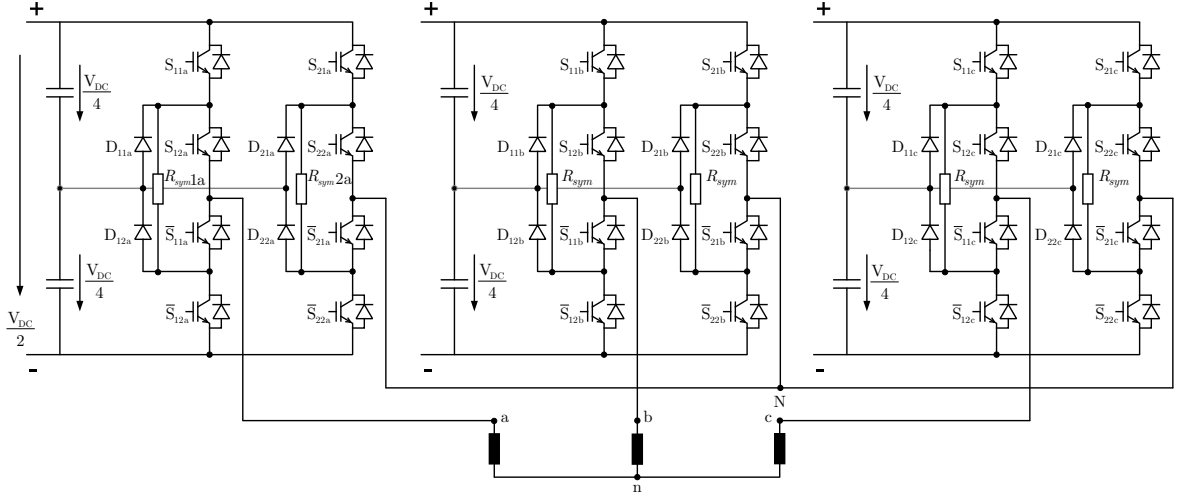


Figure 4.6.: H-bridge Neutral Point Clamped VSC [115]

The advantage is that the output voltage and therefore the input current are doubled compared with the NPC converter. This leads also to lower $\frac{dV}{dt}$ due to the five-level output voltage and the required output filter is also smaller [118]. However, double the number of devices is required for the converter construction.

In order to optimize the output voltage levels, instead of a half-bridge NPC leg, a two-level half-bridge with double the semiconductor devices voltage rating can be used. The converter devices number is reduced for the same number of output levels, improvement paid in redundancy elimination and unsymmetrical construction [119]. Similar to the two-level CHB converter, the cascade can be constructed also with three-level building blocks [116] or combination of both.

The H-bridge Neutral Point Clamped converter (Fig. 4.6) has the following advantages and disadvantages:

Advantages:

- + high efficiency
- + double output voltage
 - lower battery nominal voltage
 - reduced output filter size

Disadvantages:

- unequal loss distribution in devices
- increased number of components
 - higher overall FIT rate
- increased control complexity when different battery is used for each converter phase
- unequalized devices voltage stress → symmetry resistors are necessary

4.5. Flying Capacitor Converter

With roots from 1970's [120] and introduced in 1992 [121] as the second developed modular multilevel converter, the Flying Capacitor (FC) topology (also known as Capacitor Clamped) replaces the clamping diodes from NPC with a clamping capacitor for each converter level. The three-level structure is shown in Fig. 4.7. Two paths for zero voltage are created, paths including the flying capacitor, the converter redundancy being introduced. The redundant states for the zero voltage output must be used alternatively in order to charge and discharge the capacitor. This topology minimizes the total amount of silicon needed, improvement being paid in a increased cost of the installed capacitors.

The flying capacitor topology can be seen as a modular converter, also known as multi-cell converter [122], the building block composed of two series connected switches with a flying capacitor in parallel. Even if it can be considered as a modular converter, there is no symmetry like in CHB converter. The flying capacitors are charged with different voltages and therefore the capacitor dimensions will increase as the number of levels is increased.

Phase-shift PWM (PS-PWM) is well applied to the flying capacitor converters since the natural balance of the flying capacitors is achieved. However, this modulation strategy produces an increased line-to-line voltage ripple which results in an increased output smoothing inductor. The main drawback of this topology is the flying capacitor size which is inverse proportional with the switching frequency. Also the operation at light load will not ensure a correct voltage balancing of the flying capacitor; additional passive networks must be connected in parallel with the load for improvements [122].

The FC converter (Fig. 4.7) has the following advantages and disadvantages:

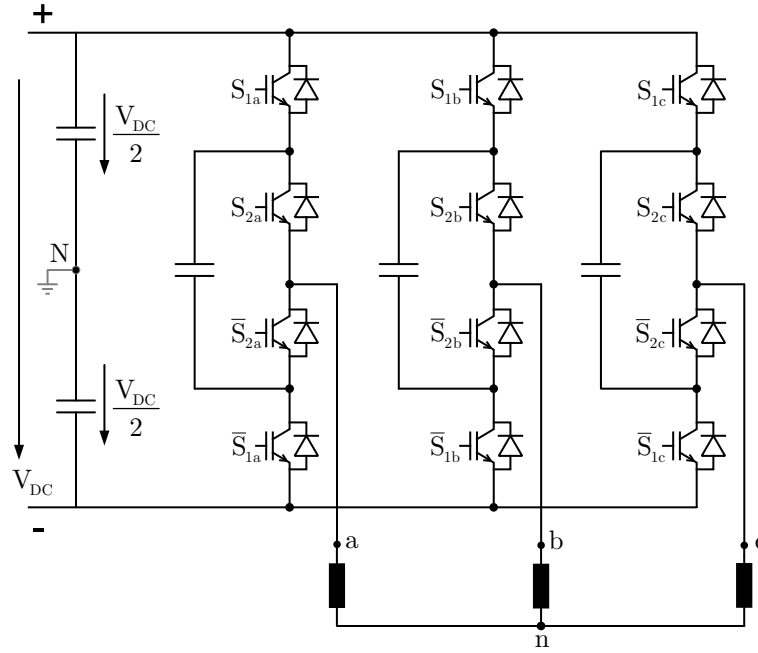


Figure 4.7.: Three-level Flying Capacitor VSC [121]

Advantages:

- + modularity of active devices
- + output redundancy
 - proportional to the number of levels
- + even devices loss distribution
 - good silicon utilization

Disadvantages:

- size of flying capacitors
 - inverse proportional with the operating switching frequency
- voltage balancing of the flying capacitors must be ensured
 - poor behaviour at light load operation
- for increased number of levels
 - asymmetrical capacitors voltages
 - difficult voltage balancing of flying capacitors

To overcome the main drawback of the hard-switch FC converter and decrease its flying capacitor size, high switching frequency operation is required. Using soft-switch technology, the switching frequency can be increased due to nearly eliminated switching losses. The utilisation of the ARCP [106] to FC converter was studied, and the ARCP FC multilevel converter was introduced [123]. Fig. 4.8 shows the three-level configuration. Apart from the flying capacitor's size reduction, the increase of the switching frequency will reduce also the output filter size. Furthermore, the ARCP design remains the same

like in the two-level approach and the converter modularity is not affected [112].

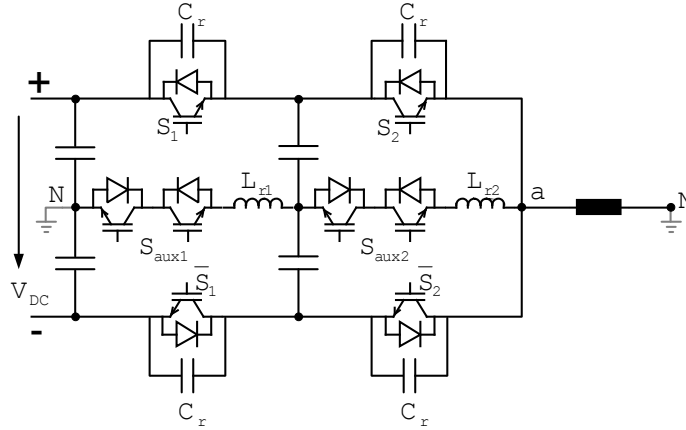


Figure 4.8.: Three-level ARCP FC VSC phase leg [123]

The soft-switch FC converter (Fig. 4.8) has the following advantages and disadvantages:

Advantages:

- + reduced switching losses
 - possibility to increase efficiency
 - reduced ratings for the main switches
- + increased switching frequency operation becomes feasible
 - output filter reduction
 - decrease size of flying capacitors

Disadvantages:

- poor auxiliary switches utilization
 - high peak currents
- losses in the auxiliary circuit
- increased number of components
 - higher overall FIT rate
 - increased converter size
- increased control complexity

4.6. Active Neutral Point Clamped Converter

The Active Neutral Point Clamped (ANPC) VSC is a derivative of NPC VSC , topology presented in Fig. 4.9. Adding two additional transistors in anti-parallel with the clamping diodes, two bidirectional current paths for the zero voltage vectors are created. Having two paths for zero voltage the converter has redundancy and the loss of the NPC stressed devices can be taken over by the active switches, improving the overall loss distribution [111]. Furthermore, partial modularity in the converter construction is achieved having the two-level half-bridge converter as building block.

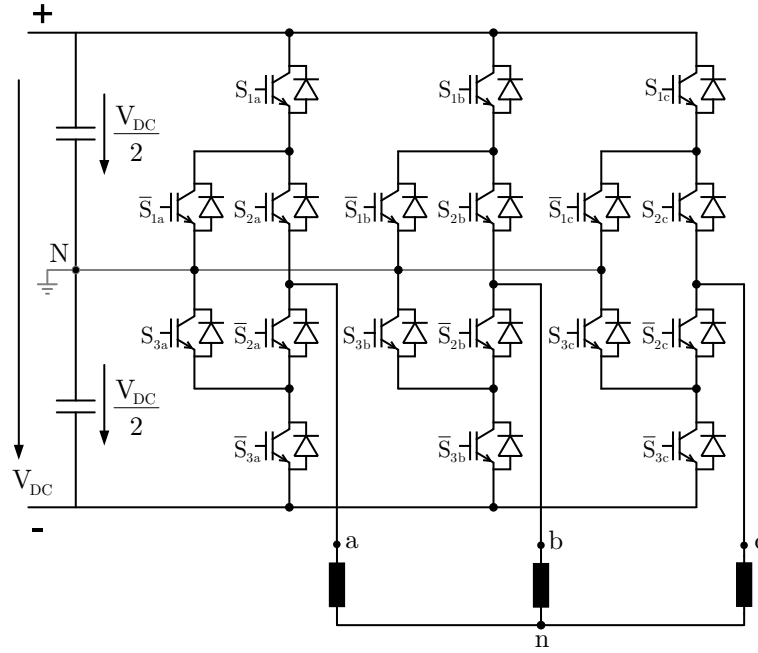


Figure 4.9.: Three-level Active Neutral Point Clamped VSC [111]

Firstly, the active transistors were introduced to achieve the equal voltage sharing between the serial connected outer and inner switches [124]. A similar topology was presented to achieve three-level soft-switch [125]. Later on, the ANPC was introduced in [111] making use of the active transistors to redistribute the losses from the most stressed devices in NPC.

The ANPC converter (Fig. 4.9) has the following advantages and disadvantages:

Advantages:

- + redundancy for the 0 V switching state
 - equalized devices thermal stress
 - increased reliability → possibility for 0 V state on-line reconfiguration
- + equalized devices voltage stress
- + partial modularity
- + high efficiency

Disadvantages:

- increased number of components
 - increased price
- increased control complexity

The modulation of the ANPC converter is an extension of the NPC converter, basically all the NPC control strategies can be implemented on this converter. Furthermore, the redundancy for zero voltage vectors is used to achieve even loss distribution. Natural

doubling of the apparent switching frequency can be achieved also, advantage for the single phase applications only. For the high power three-phase applications, the filter size is increased because of the high voltage ripple on the line voltage generated by the phase-shifted modulation technique.

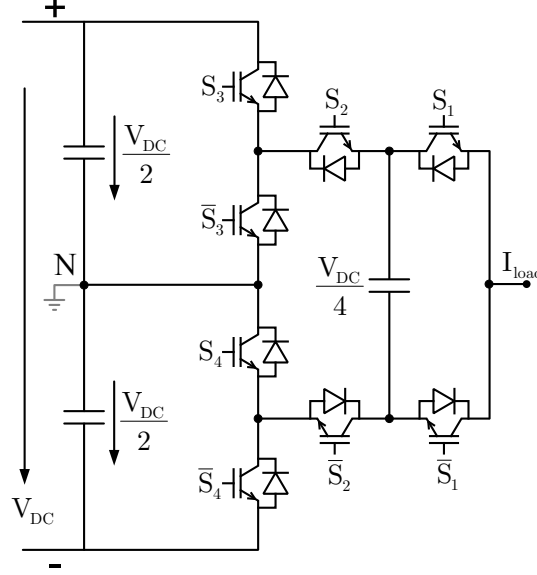


Figure 4.10.: Five-level Active Neutral Point Clamped VSC phase leg [126]

An extension to the three-level ANPC is represented in Fig. 4.10, the Five-level Active Neutral Point Clamped VSC introduced in 2005 [126]. It is a combination between three-level ANPC (Fig. 4.9) and the FC converter (Fig. 4.7). With the addition of the FC cell, an intermediate level is created in comparison with ANPC converter and the output redundancy is enhanced. Switches ($[S_1, \bar{S}_1]$ and $[S_2, \bar{S}_2]$) are designed to block $\frac{1}{4}$ of the DC-link voltage while the switches ($[S_3, \bar{S}_3]$ and $[S_4, \bar{S}_4]$) are designed to block $\frac{1}{2}$ of the DC-link voltage. The topology can be generalized to n levels [126].

An important advantage for the five-level ANPC converter is the reduced number of devices in conduction per state, from four devices to three. However, the drawbacks of the FC converter still exist, but in this case the capacitor voltage rating is minimized to the half ($\frac{V_{DC}}{4}$) as required to three-level FC ($\frac{V_{DC}}{2}$). The operation with light load is still poor; the capacitor voltage balancing cannot be achieved without additional components, like in the FC VSC [122].

The five-level ANPC converter (Fig. 4.10) has the following advantages and disadvantages:

Advantages:	Disadvantages:
+ high output redundancy → smaller output filter	- flying capacitors size → inverse proportional with the switching frequency of $[S_1, \overline{S_1}]$ and $[S_2, \overline{S_2}]$
+ reduced number of devices in conduction → lower conduction losses	- flying capacitors voltage balancing must be ensured
+ hybrid devices can be used → high efficiency	→ poor behavior at light load operation

4.7. Cascaded half-bridge Converter

One of the most important hybrid concept is the combination of the CHB (Fig. 4.1) and FC (Fig. 4.7) converters, in the so-called Modular Multilevel Converter (MMC/M2C). It is based on cascaded two-level half-bridge cells (ChB), patented in [127] and introduced in [128]. The schematic is presented in Fig. 4.11. Due to its highly modular construction and theoretically unlimited blocking voltage capability, this topology is suitable for medium and especially for high voltage grid application [129]. The centralized DC-link energy storage elements are moved to decentralized DC-links, this being an advantage considering its maintenance and disadvantage considering the total installed capacitors.

Two coupled or uncoupled arm inductors need to be installed in each converter phase, to limit the cells capacitors charging and discharging current. When the arm inductors value is large, the converter behaviour is as a current source. When the arm inductors value is small or when there is a coupling between them the converter behaviour is as a voltage source [129]. Several control methods were proposed to control and reduce the circulating current present in the converter arms [130, 131].

The converter construction is based on optimized IGBT's for low conduction loss and operation with low and very low switching frequency. The modular construction allows the achievement of low DC-links stray inductance due to decentralized capacitors. Low frequency PWM methods are usually applied for this topology. Whereas the number of converter modules is high enough, the staircase modulation based on harmonic elimination method can be applied for minimum converter switching loss [101]. However, the applied approach must ensure balance in the converter cell voltages [129, 128].

The ChB converter (Fig. 4.11) has the following advantages and disadvantages:

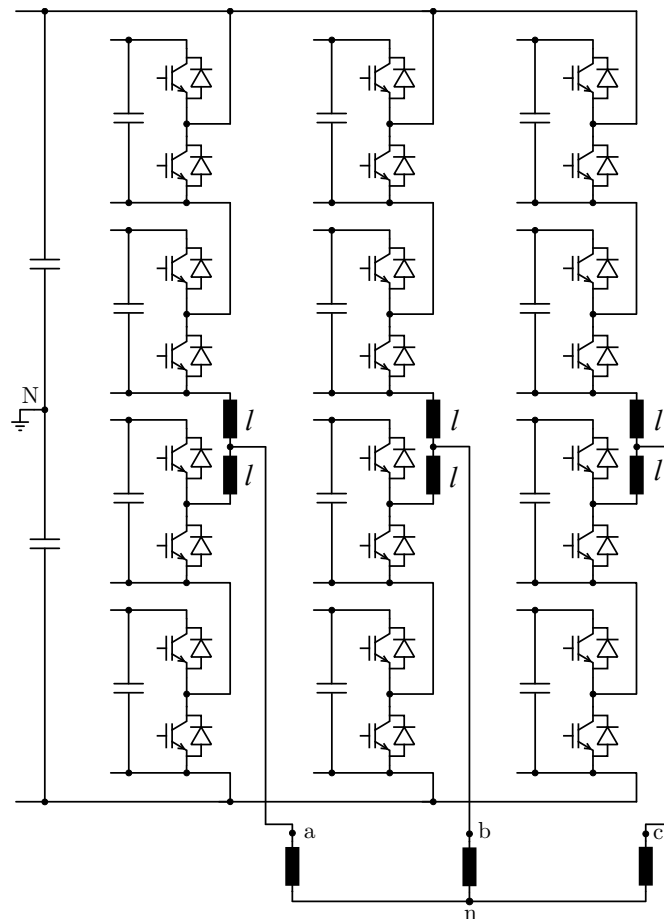


Figure 4.11.: Cascaded half-bridge Converter [127]

Advantages:

- + highest degree of modularity
 - highest design flexibility
 - usage of mature semiconductors
- + good failure management
 - cell bypass for design with high number of cells [132]
 - device bypass for series connected devices within a cell [133]
- + simple and robust construction
- + very small or no output filter

Disadvantages:

- first and second harmonic current ripple on the cells capacitors
- circulating current in each phase
- high number of active devices
 - high number of gate drivers and control signals

4.8. Summary

A survey on multilevel converters for medium voltage was given in this chapter. Hard-switched and soft-switched converter topologies were presented for the considered cascaded and clamped structures. Advantages and disadvantages are given for each topology, facts that can support future selection and evaluations.

In order to compare further the presented converter topologies, apart from the mentioned advantages and disadvantages, it is relevant to consider the number of required components for construction. On one hand, this is relevant for the converters reliability. The higher the number of used components, the higher the possible overall failure in time (FIT) rate becomes. On the other hand, the number of components has also an effect on the construction price. However, the cost function is particular for each converter topology, for each implementation procedure and dependent on the possibility of components mass production.

The summarized components for the considered converter topologies are presented in Table 4.1. Assuming equal voltage drops for all phases on the grid impedance (Z_g) and output filter impedance (Z_f), the reference DC-link voltage (V_{DC}) is calculated taken as for the three-phase two-level approach, voltage given by equation 4.1:

$$V_{DC} = V_{g,LL,pk,max} + I_{g,pk,max} \cdot (Z_f + Z_g) \quad (4.1)$$

Here, $V_{g,LL,pk,max}$ and $I_{g,pk,max}$ are the maximum peak values for the line-to-line grid voltage and grid current respectively. This is valid only considering the modulation with injection of the third harmonic equivalent to SVM for the given rated power transfer.

Having this, the converters number of semiconductor devices with the operating blocking voltage, number of necessary capacitors and isolated DC sources for nominal voltage as well as auxiliary components for resonant topologies are given in Table 4.1.

The maximum devices blocking voltage and their rated and operating current are chosen with regard to the implementation and desired converter lifetime. It must be noticed that for the converter solutions based on H-bridge (two-level and three-level), the number of required isolated DC sources can be reduced when a transformer with open windings is installed in the output. However, if lower current is desired in the DC-link, it is worth to use isolated sources which can be provided in the application of battery energy storage.

DC-AC	LVL	Switches	Diodes	Capacitors	DC sources	Auxiliaries		
	N	$n \times V_{\text{block}}$	$n \times V_{\text{block}}$	$n \times V_{\text{nom}}$	$n \times V_{\text{nom}}$	S_{aux}	L_{r}	C_{r}
CHB	3	$12 \times V_{\text{DC}}/2$	—	$3 \times V_{\text{DC}}/2$	$3 \times V_{\text{DC}}/2$	—		
	5	$24 \times V_{\text{DC}}/4$	—	$6 \times V_{\text{DC}}/4$	$6 \times V_{\text{DC}}/4$	—		
	7	$36 \times V_{\text{DC}}/6$	—	$9 \times V_{\text{DC}}/6$	$9 \times V_{\text{DC}}/6$	—		
ACHB	7	$12 \times V_{\text{DC}}/3$	—	$3 \times V_{\text{DC}}/3$	$3 \times V_{\text{DC}}/3$	—		
		$12 \times V_{\text{DC}}/6$		$3 \times V_{\text{DC}}/6$	$3 \times V_{\text{DC}}/6$			
	9	$12 \times 3V_{\text{DC}}/8$	—	$3 \times 3V_{\text{DC}}/8$	$3 \times 3V_{\text{DC}}/8$	—		
		$12 \times V_{\text{DC}}/8$		$3 \times V_{\text{DC}}/8$	$3 \times V_{\text{DC}}/8$			
ARCP	3	$12 \times V_{\text{DC}}/2$	—	$6 \times V_{\text{DC}}/4$	$3 \times V_{\text{DC}}/2$	12 6 12		
CHB	5	$24 \times V_{\text{DC}}/4$	—	$12 \times V_{\text{DC}}/8$	$6 \times V_{\text{DC}}/4$	24 12 24		
NPC	3	$12 \times V_{\text{DC}}/2$	$6 \times V_{\text{DC}}/2$	$2 \times V_{\text{DC}}/2$	$1 \times V_{\text{DC}}$	—		
	4	$18 \times V_{\text{DC}}/3$	$12 \times 2V_{\text{DC}}/3$	$3 \times V_{\text{DC}}/3$	$1 \times V_{\text{DC}}$	—		
	5	$24 \times V_{\text{DC}}/4$	$36 \times V_{\text{DC}}/4$	$4 \times V_{\text{DC}}/4$	$1 \times V_{\text{DC}}$	—		
ARCP NPC	3	$12 \times V_{\text{DC}}/2$	$6 \times V_{\text{DC}}/2$	$4 \times V_{\text{DC}}/4$	$1 \times V_{\text{DC}}$	12 3 9		
HNPC	5	$24 \times V_{\text{DC}}/4$	$12 \times V_{\text{DC}}/4$	$6 \times V_{\text{DC}}/4$	$3 \times V_{\text{DC}}/2$	—		
FC	3	$12 \times V_{\text{DC}}/2$	—	$5 \times V_{\text{DC}}/2$	$1 \times V_{\text{DC}}$	—		
	4	$18 \times V_{\text{DC}}/3$	—	$6 \times V_{\text{DC}}/3$	$1 \times V_{\text{DC}}$	—		
				$3 \times 2V_{\text{DC}}/3$				
	5	$24 \times V_{\text{DC}}/4$	—	$3 \times V_{\text{DC}}/2$	$1 \times V_{\text{DC}}$	—		
				$3 \times 3V_{\text{DC}}/4$ $7 \times V_{\text{DC}}/4$				
ARCP FC	3	$12 \times V_{\text{DC}}/2$	—	$2 \times V_{\text{DC}}/2$ $6 \times V_{\text{DC}}/4$	$1 \times V_{\text{DC}}$	12 6 12		
ANPC	3	$18 \times V_{\text{DC}}/2$	—	$2 \times V_{\text{DC}}/2$	$1 \times V_{\text{DC}}$	—		
	5	$12 \times V_{\text{DC}}/2$	—	$2 \times V_{\text{DC}}/2$	$1 \times V_{\text{DC}}$	—		
		$12 \times V_{\text{DC}}/4$		$3 \times V_{\text{DC}}/4$				
ChB	3	$24 \times V_{\text{DC}}/2$	—	$12 \times V_{\text{DC}}/2$	$1 \times V_{\text{DC}}$	—		
(M2C)	4	$36 \times V_{\text{DC}}/3$	—	$18 \times V_{\text{DC}}/3$	$1 \times V_{\text{DC}}$	—		
	5	$48 \times V_{\text{DC}}/4$	—	$24 \times V_{\text{DC}}/4$	$1 \times V_{\text{DC}}$	—		

Table 4.1.: Multilevel DC-AC converters necessary components and voltage ratings

Chapter 5.

Single-Stage Medium Voltage Grid Converters for Energy Storage

This chapter presents the five-level CHB, three-level NPC, ANPC and FC converters as power electronic interfaces for single-stage grid connection of HV battery systems. A simulation-based converter topologies comparison is given in terms of efficiency, common mode voltage, passive components and redundancy for a 6 kV battery system with the rated power of 5 MVA

5.1. Introduction

The increase of solar and wind systems in the recent years is exponential, and the growth in installed capacity is already planned [134]. The disadvantage of these energy sources, especially for wind farms, is the wide fluctuation of output power depending on the weather conditions. This output power variation is reflected in frequency and voltage fluctuations on the load bus [135, 136]. Therefore, the integration of renewable energy systems in the power system network is still a challenge in our days. To overcome this, storage systems connected to the electricity grid can smooth the output power of wind farms by acting as a load/generator improving the grid stability and power quality. Battery energy storage systems (BESS) represent a versatile solution for storage with high efficiency, high power, long possible energy demand and fast response.

In order to connect BESS to the grid, different power converter topologies are available. Basically the main classification can be done in two groups: single-stage and two-stage. Two-stage topologies with intermediary DC-DC converter, shown in Fig. 5.2, decouple the batteries from the DC-AC conversion stage and this brings benefits to batteries. However, the conversion efficiency is decreased due to the losses in the DC-DC converter. Therefore using single-stage topologies, shown in Fig. 5.1, where the batteries are directly connected to the inverter DC-link, the efficiency can be increased. This improvement in efficiency brings the disadvantage of having a floating voltage in the inverter's DC-link dependent on the batteries characteristic. As a consequence, the battery pack nominal

voltage must be dimensioned somewhat higher (depending on the technology) to be able to inject current in the grid until the batteries are discharged up to the desired level.

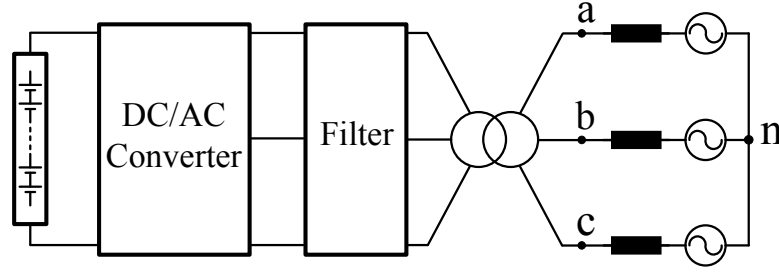


Figure 5.1.: Single stage general grid converter topology

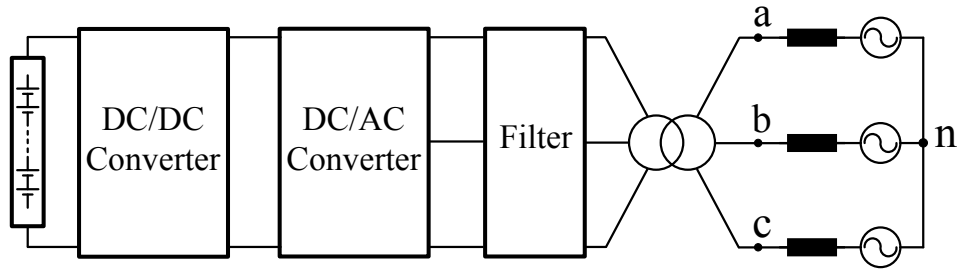


Figure 5.2.: Two stage general grid converter topology

For low voltage storage applications, the classical two-level converter is the most used topology [137]. Its control simplicity is outstanding but has important drawbacks like: common mode voltage up to half of the DC-Link voltage, high switching frequency operation and large output filter in order to comply with harmonic standards. When the operating voltage is increased, this topology requires series connected power semiconductors which complicates the design, increases the electromagnetic interference and therefore the topology is not interesting anymore. For medium voltage, the multilevel converters are the key technology. It was shown that even for low voltage applications, three-level converters are more efficient compared with the classical two-level converters [138].

Multilevel converters represent a smart way to connect power semiconductors in series, decreasing the voltage ripple and the output harmonic distortion as well as the common mode voltage. To achieve equivalent voltage spectrum with the two-level converter the switching frequency is decreased, therefore these converters are more suitable for applications where high currents are switched. The first two topologies were introduced in 1970's, the Cascaded H-Bridge (CHB) converter [99, 100], followed by the Neutral Point Clamped (NPC) converter [107]. By clamping capacitors instead of diodes, the Flying Capacitor (FC) converter was introduced in 1992 [121]. An improved version of NPC converter was introduced in 2001, the Active Neutral Point Clamped (ANPC) converter [111]. Various hybrid topologies were lately introduced, based on the main

Rated power	S	5 MVA
Rated AC grid line voltage	$V_{g,LL}$	10/20 kV
Rated AC grid frequency	f	50 Hz
Output transformer	$\frac{V_s}{V_p}$	$\frac{10/20 \text{ kV}}{4.16 \text{ kV}}$
Rated converter line voltage	$V_{c,LL}$	4.16 kV
Rated converter RMS current	I	694 A
Power factor	PF	$0.95_{leading} - 0.95_{lagging}$
Harmonic standard		EN 61000-2-4

Table 5.1.: Converter's imposed basic parameters

concepts presented above, one of the most important ones being the five-level ANPC [126].

High power single-stage converters topologies for energy storage gained the interest in industry in the last years, coupling HV batteries to the medium and high voltage grids. The 40 MW battery energy storage system was installed in Alaska [117] in 2003, with power electronic conversion system based on interleaved H-bridge NPC converters. For a 5 MW system with lithium ion batteries, the single-stage NPC topology was used for voltage and frequency regulation [109].

Four converter topologies are considered here, the five-level CHB (Fig. 4.1), three-level NPC (Fig. 4.4), three-level ANPC (Fig. 4.9) and three-level FC (Fig. 4.7) converters, as interfaces for direct connection of batteries to the medium voltage AC grid. The rated power is 5 MVA. The choice is justified considering the number of passive and active components, capacitors voltage balancing, silicon utilization and control complexity [139].

5.2. Converter specifications

Summary of the converters required number of components and their voltage ratings were given in Table 4.1. Considering the imposed parameters from Table 5.1, the converter necessary DC-link voltage has to be established.

In single stage topologies the converter DC-link voltage has to withstand the batteries voltage variations and has to adapt the charging and discharging voltage according to the battery state of charge. This voltage charge and discharge characteristics is depend on the used battery technology, differs from one technology to another and is also dependent on the batteries temperature. Flooded lead-acid batteries will be considered, this being a mature technology presenting satisfactory performances for a low price, technology

which was applied for spinning reserve and frequency control [140, 141]. For this battery technology the considered voltage variation was about 15% depending on the state of charge [142], considering a 50% maximum depth of discharge (DOD) which is optimum as a cost function for this technology. Thus, the battery voltage taken when the discharge is completed will define the number of batteries in the system in order to be able to inject the nominal power in grid, this being given by Eq. 5.1:

$$V_{bat,min} = \sqrt{2} \cdot V_{LL,PCC} = \sqrt{2} \cdot 4.16 = 5.88 \text{ kV} \quad (5.1)$$

The voltage drop on the grid impedance, this will not be considered for now since the HV to MV transformers introduced impedance is around 1 mΩ [143]. The sum of the transformers introduced impedance, which is mostly inductive, will be further considered to determine the necessary filtering to comply with the considered standard harmonic distortion limits. Considering an increased voltage at full charge of about 15%, and a necessary safety margin of 10%, results the maximum DC-link voltage:

$$V_{DC,max} = 1.25 \cdot \sqrt{2} \cdot V_{LL,PCC} = 7.35 \text{ kV} \quad (5.2)$$

Thus, for the considered three-level topologies the DC-link voltage will be imposed by the battery voltage and the modulation index has to adapt the output voltage in order to charge or discharge the batteries. For this purpose, the space vector pulse width modulation (SV-PWM) is considered to have the best utilization of the DC-Link. A maximum theoretical modulation index close to 1.15 is imposed when the batteries are almost at 50% DOD. Unlike the three-level topologies, the CHB topology divides the battery bank voltage in 4 to be used for each converter cell. This is a good advantage for this topology; lower voltage devices can be used and a redundant cell can improve the converter reliability. However, disadvantages arises when the batteries are connected to the H-Bridge cell, the 2nd harmonic ripple is seen at the batteries terminals through the cell capacitor.

5.3. Semiconductors requirements

The amount of silicon in the converter design is a trade-off which takes into consideration the total installed switch power, converter losses and desired converter lifetime. In Table 5.2 the semiconductors specifications are summarized. The selection was based on the available modules available on the market in March 2010, which comply with the converter requirements. Thus, for the three-level (3L) NPC, ANPC and FC converters the 6.5 kV IGBT (FZ750R65KE3) from Infineon was considered with a nominal current of 750 A and the 3.3 kV IGBT (FZ800R33KL2C) for the five-level (5L) CHB converter with a nominal current of 800 A. The assumed heatsink temperatures is $T_h = 80 \text{ °C}$ to be controlled by other means, the maximum junction temperature is $T_{j,max} = 125 \text{ °C}$. The maximum switching frequency is $f_{sw,max} = 1050 \text{ Hz}$.

		3L-NPC	3L-ANPC	3L-FC	5L-CHB
$V_{DC,max}$	[V]	7350	7350	7350	1837
$V_{CE,n}$	[V]	6500	6500	6500	3300
$V_{com,max}$	[V]	3675	3675	3675	1837
$I_{c,n}$	[A]	750	750	750	800
$V_{CE(sat),typ}$	[V]	4.3	4.3	4.3	3
S_S	[MVA]	73.125	87.75	58.5	63.36

Table 5.2.: Semiconductors requirements for single stage MV converters

It can be noticed from Table 5.2 that the lowest installed switch power is required for the FC converter, this topology having the best usage of the silicon area. More interesting is to see the low installed switch power for the CHB converter, lower than NPC. Must be noted that there is also an overrating in current compared with the other converter topologies (800 A compared with 750 A). All topologies are slightly underrated in voltage, considering that the overall system functionality at the highest DC-link voltages is only for a short time when the state of charge approaches 100%.

In the ideal case the required devices current rating for the considered topologies will differ for the four quadrant converter operation, therefore the differences will show a different loss distribution and magnitudes for the restricted ratings. The devices deadtime considered for the most critical fall times were chosen to be 8 μ s for the 6.5 kV IGBT and 5 μ s for the 3.3 kV IGBT .

Considering the present application the switches overrating is not desired. The system lifetime is limited by the battery technology which is expected to last for 1 to 4 years depending on the usage [8]. The total installed switch power (S_S) is given in equation Eq. 5.3, for n IGBT modules (transistors with antiparallel diodes) and m diodes which are considered with a typical half silicon area of an IGBT :

$$S_S = V_{CE,n} \cdot I_{C,n} \cdot n + 0.5 \cdot V_{RRM} \cdot I_{F,n} \cdot m \quad (5.3)$$

5.4. Design of passive components

5.4.1. Output filter design

The L output filter will be considered in this study to determine the necessary current ripple reduction for the output current to comply with the maximum of 5% THD at full

power and 8% THD imposed by the EN 61000-2-4 over the entire operation range. The maximum ripple current is defined by Eq. 5.4 [144]:

$$\Delta I_{max} = \frac{1}{n} \cdot \frac{V_{DC}}{L_f \cdot f_{sw}} \quad (5.4)$$

where the factor n varies with the number of output voltages, 2 for two-level, 4 for three-level and 6 for five-levels.

The grid impedance has to be considered as well, and it can be estimated by the 20 kV to 4.16 kV short-circuit impedance calculated with Eq. 5.5:

$$z_k = \frac{v_k \cdot V_p}{\frac{S_n}{\sqrt{3} \cdot V_s} \cdot n^2} \quad (5.5)$$

where V_p is the primary winding voltage (4.16 kV), V_s secondary winding voltage (20 kV), v_k the short circuit voltage, S_n the nominal power and n the transformation ratio. Assuming a 5% short-circuit voltage, the short-circuit impedance is 12.76 mΩ. Thus, considering also the HV to MV transformer impedance of around 1 mΩ and a typical R/X ratio of 0.1 the grid inductance for 50 Hz grid is found to be $L_g = 43.58 \mu\text{H}$.

Taking the most critical operation point ($V_{DC,max}$), and choosing the converters switching frequency, the necessary filtering inductances are presented in Table 5.3. It can be noticed that the CHB has the smallest necessary filtering inductor while keeping the installed power smaller than NPC. It must also be noticed the reduced switching frequency and increased filter size of the ANPC, due to the applied phase shifted PWM strategy.

		3L-NPC	3L-ANPC	3L-FC	5L-CHB
f_{sw}	[Hz]	1050	550	1050	550
L_f	[μH]	1230	3250	1720	980

Table 5.3.: Converters switching frequency and necessary filtering

5.4.2. Design of flying capacitors

The flying capacitors size is inverse proportional with the commutation frequency, this being the main drawback of this topology. Even if the converter output frequency is doubled compared with the switching frequency like in ANPC converter [145], the switching frequency has to be kept high enough to minimize the capacitance. The capacitors size is approximated with the following equation:

$$C = \frac{I_{ph,RMS}}{p \cdot \Delta V_C \cdot f_{sw}} \quad (5.6)$$

where p is the number of flying capacitor cells, and ΔV_C is the maximum voltage ripple. Thus, for a maximum ripple of 10% of the maximum capacitor voltage $V_{DC,max}/2$, the calculated capacitance is 900 μF .

5.4.3. DC-link capacitors size

The sizing of the DC-link capacitors, and the chosen capacitors technology to be used is a very important aspect. Standard power converters are designed with electrolytic capacitors, which provide high energy storage density. However, these are the components which are the first to be replaced during the maintenance schedule. Therefore, film capacitors are considered instead to improve the reliability of the DC-link [89]. This implies the reduction of installed capacity and thus the decoupling of the power source and load is reduced, and the control needs to be adapted for these conditions.

A general approach to choose the minimum DC-link capacitor value, is given in Eq. 5.7 [86]:

$$C_{\min} = \frac{\Delta Q_{C,\max}}{\Delta V_{DC,\max}} = \frac{\max \left(\int (i_C - i_{C,avg}) dt \right)}{\Delta V_{DC,\max}} \quad (5.7)$$

Here, $\Delta Q_{C,\max}$ is the maximum capacitor charge variation, which is given by the capacitor current ripple apart from the current drawn by the capacitor itself (e.g. power loss in the parasitic equivalent series resistance).

For the considered three-level converter topologies, the DC-link capacitors sizing is similar. The maximum allowed bus ripple must be reduced for the 6th harmonic and considerations must be done in the case of 2nd harmonic ripple during grid voltage unbalance. The highest installed DC-link capacity is required for the five-level CHB converter, to reduce the 2nd harmonic current. This is normally drawn by the H-bridges from each battery bank.

5.5. Simulation results

Converter models were implemented in Matlab/Simulink, and the power circuit including the thermal model were implemented using PLECS blockset under the same programming environment. The SV-PWM technique was used, with level-shift for NPC and phase-shift PWM for the other topologies. For a better view of the reference(s) and carriers, the natural sampling technique is used here. Implementations at the required power level will require double edge sampling or oversampling (in case of very low switching frequency).

5.5.1. Converters output voltages

In Fig. 5.3 the output voltages for the three-level NPC converter are presented for the considered switching frequency of 1050 Hz, the same frequency as the output voltage.

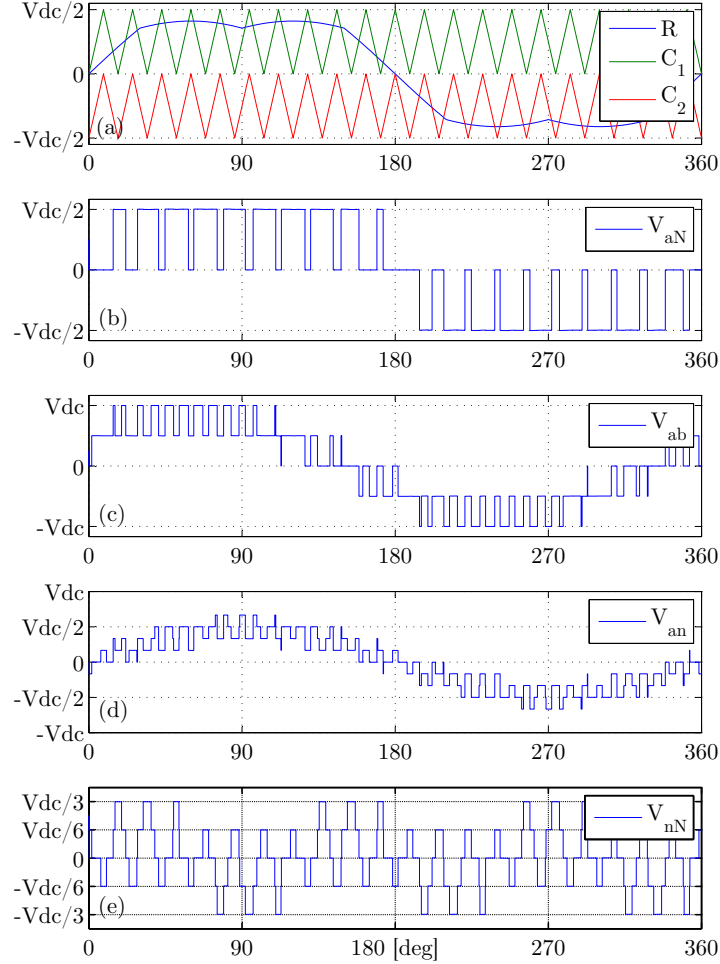


Figure 5.3.: Three-level NPC converter output waveforms

Fig. 5.3.(a) shows the reference and the level shifted carriers, Fig. 5.3.(b) shows the phase a to DC-link midpoint (neutral) voltage, Fig. 5.3.(c) shows the line to line voltage, Fig. 5.3.(d) shows the phase a load voltage (phase to grid isolated neutral) and Fig. 5.3.(e) shows the common mode voltage.

The main advantage of the level-shift PWM (LS-PWM) over the phase-shift PWM (PS-PWM) for the considered three-phase converter circuits, can be noticed by comparing the output line voltage with the ones from ANPC and FC converters, the ripple is minimized to $V_{DC}/2$.

In Fig. 5.4 the output voltages for the three-level ANPC converter are presented for the considered switching frequency of 550 Hz, using PS-PWM. Fig. 5.4.(a) shows the reference

and the phase shifted carriers, Fig. 5.4.(b) shows the phase a to DC-link neutral voltage, Fig. 5.4.(c) shows the line to line voltage, Fig. 5.4.(d) shows the phase a load voltage and Fig. 5.4.(e) shows the common mode voltage.

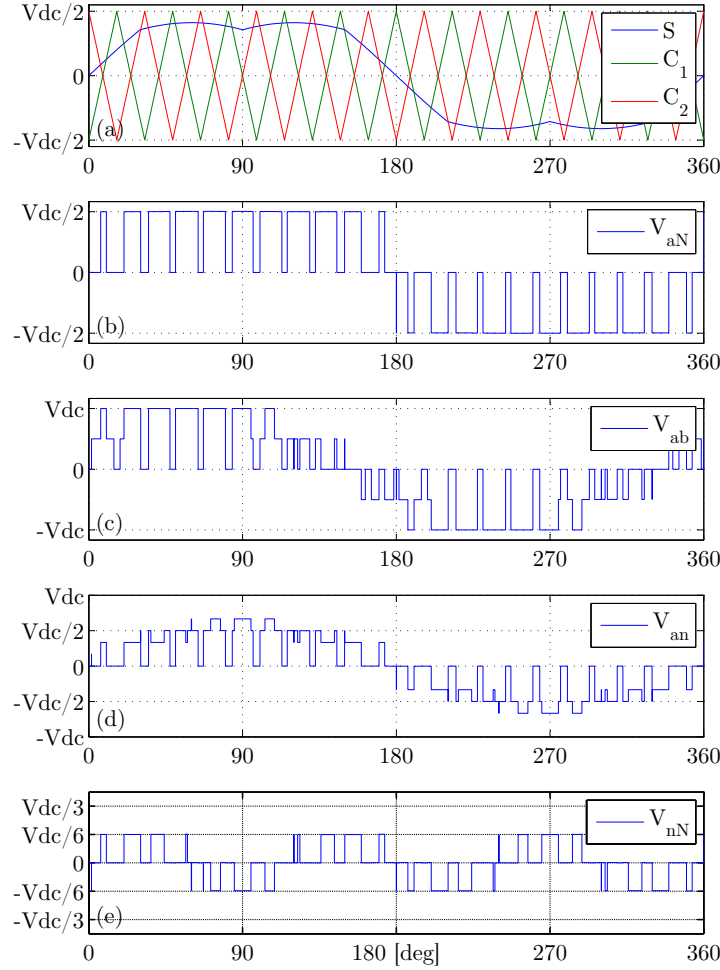


Figure 5.4.: Three-level ANPC converter output waveforms

Higher line to line ripple can be seen for the ANPC converter, up to V_{DC} , when using PS-PWM. This will lead to an increased required output filter, as seen in Table 5.3, to comply with the harmonic requirements imposed by grid connection standards. However, the ANPC converter can be switched in the same as the NPC converter using LS-PWM and making use of zero voltage redundant state to distribute the losses [111]. In that case the output voltage and the necessary filtering for both topologies will be the same as for the NPC converter.

The output voltages waveforms for the three-level FC converter are presented in Fig. 5.5 for the considered switching frequency of 1050 Hz, using PS-PWM. Fig. 5.5.(a) shows the reference and the phase shifted carriers, Fig. 5.5.(b) shows the phase a to DC-link neutral voltage, Fig. 5.5.(c) shows the line to line voltage, Fig. 5.5.(d) shows the phase

a load voltage and Fig. 5.5.(e) shows the common mode voltage.

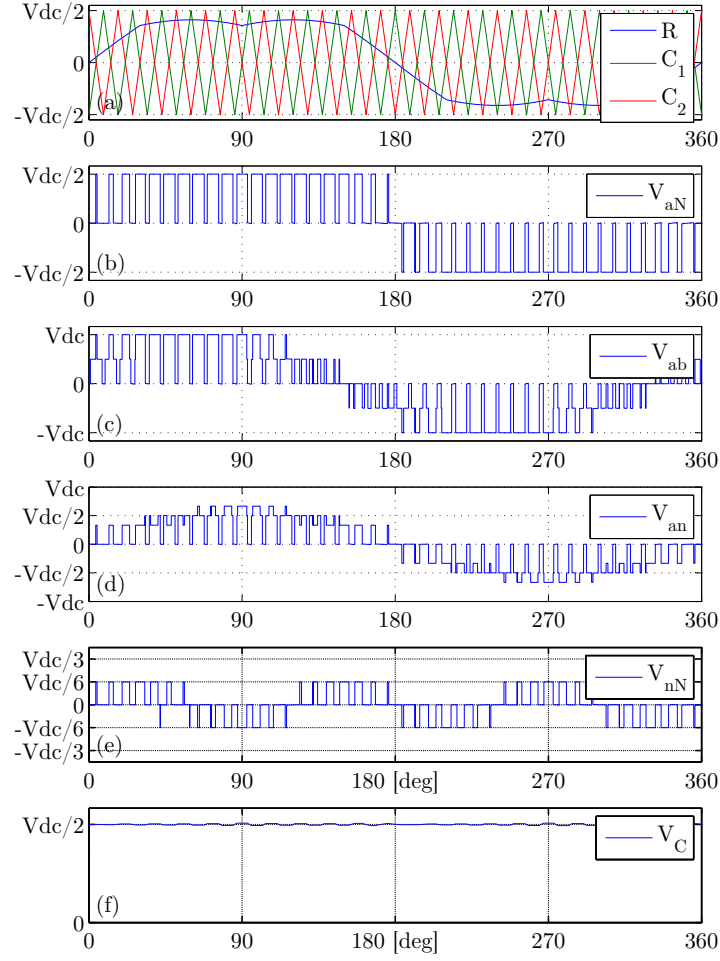


Figure 5.5.: Three-level FC converter output waveforms

Higher switching frequency is normally required, to reduce the flying capacitor size. An increased common mode voltage is observed for the LS-PWM (Fig. 5.3.(d)), going up to $V_{DC}/3$ compared to $V_{DC}/6$ for PS-PWM in Fig. 5.4.(e) and Fig. 5.5.(e). This will result in higher common mode currents through the parasitic capacitances to ground and during switching dead times.

Using the phase-shift PWM for the ANPC converter it's possible to double the apparent switching frequency of the output voltage [145], thus a reduction of switching frequency is possible similar with the three-level FC converter. Both converters have two bidirectional paths for 0 V switching state. This improvement is achieved with the expense of having a line voltage ripple up to V_{DC} , and the necessary output filter increasing as well. This can also be observed in Fig. 5.4.(d), in the phase voltage found at the load terminals. This is the phase to neutral voltage without the common mode voltage ($V_{aN} - V_{nN}$). However, this modulation strategy is suitable for the single phase ANPC converter topology.

For the five-level CHB switched with 550 Hz (see Fig. 5.6), similar control strategy is applied, phase-shifting the carrier with 180 degrees as well as the references. The result in terms of line voltage ripple is better as compared the FC converter and the PS-PWM ANPC converter, due to the increased number of levels, reduced to a maximum of $V_{DC}/2$. For the three-level CHB topology, the result will be similar to a three-level FC.

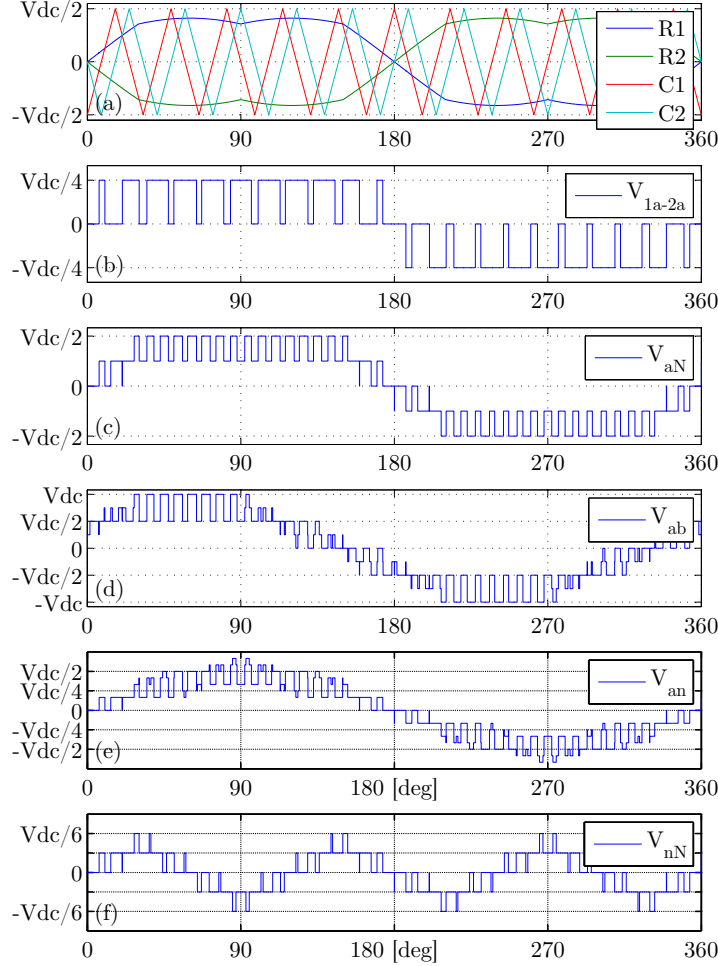


Figure 5.6.: Five-level CHB converter output waveforms

The higher output redundancy leads to the smallest output filter (see Table 5.3). This fact also improves the efficiency in the operation at unity power factor, since the required reactive power to be delivered to the output L filter is reduced.

5.5.2. Converters semiconductor loss analysis

The converter semiconductor losses were simulated for unity power factor, with the loss distribution over the entire DC-link voltage variation at the nominal rated power of 5 MW. Switching and conduction loss characteristics were taken from the datasheets

[146]. The implemented thermal model for each transistor with antiparallel diode is shown in Fig. 5.7, given in the Foster network by the manufacturer. Clamping diodes from the NPC converter are modelled with the characteristic of the IGBT antiparallel diode for symmetry.

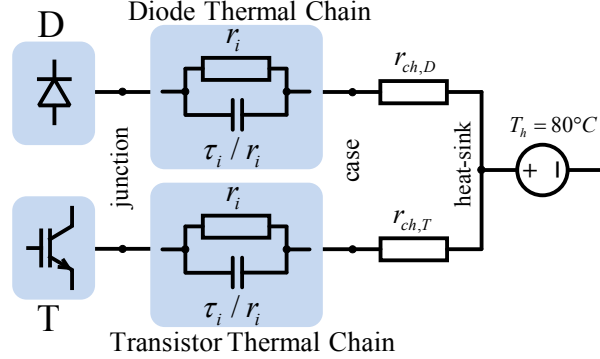


Figure 5.7.: IGBT module thermal circuit

In Fig. 5.8, Fig. 5.9, Fig. 5.10 and Fig. 5.11 the semiconductors loss characteristics for the considered converter topologies are shown, for the given DC-link voltage variation. The turn ON and turn OFF losses of all transistors are added in $P_{sw,T}$, while in $P_{sw,D}$ the recovery losses of all diodes are added.

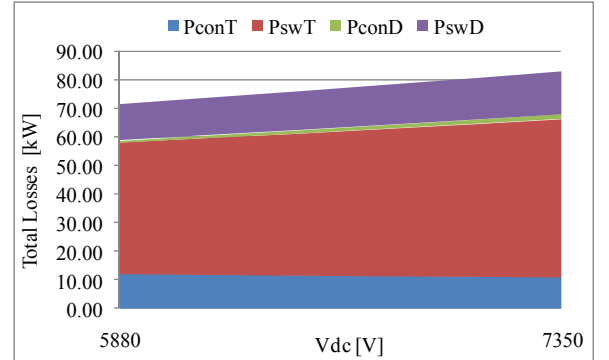
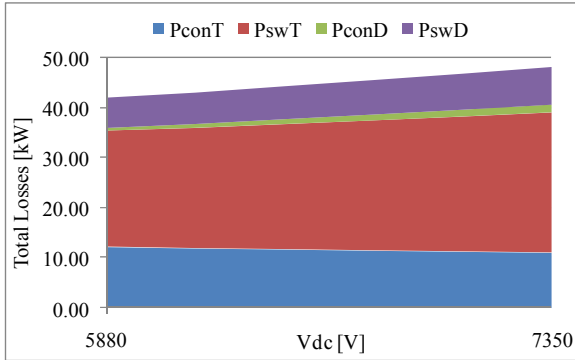


Figure 5.8.: Three-level NPC converter losses - $f_{sw} = 1050 \text{ Hz}$ Figure 5.9.: Three-level FC converter losses - $f_{sw} = 1050 \text{ Hz}$

Analysing the Fig. 5.8, it can be noticed that the switching losses are dominant and increases with the DC-link voltage increase. Conduction losses are increased for lower DC-link voltages, operation mode where the modulation index is higher to maintain the rated power transfer.

Increased switching losses for the FC converter are noticed, the average switching frequency is higher to achieve the doubled output frequency, for the same silicon area as the other three-level converters. However, this is also amplified by the under rating in voltage of the power semiconductors which was identical for the three-level topologies.

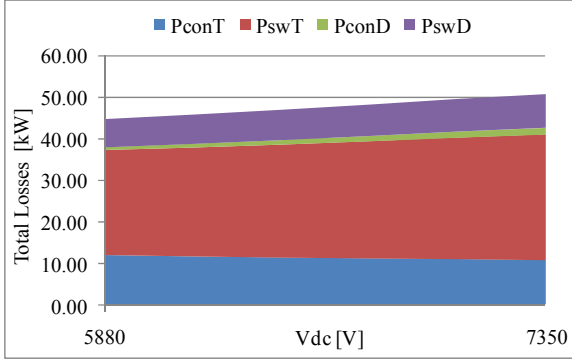


Figure 5.10.: Three-level PS-ANPC converter losses - $f_{SW} = 550 \text{ Hz}$

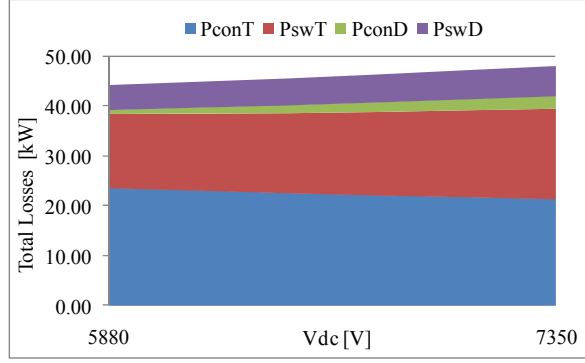


Figure 5.11.: Five-level CHB converter losses - $f_{SW} = 550 \text{ Hz}$

With the usage of the PS-PWM for the ANPC converter, higher losses are seen in Fig. 5.10 compared with NPC converter in Fig. 5.8. This is mainly because of the increased size of the output filter to comply with the grid harmonic requirements. To reduce switching losses even further, optimized modulation strategies such as SHE-PWM can be applied [147, 148].

The loss distribution for an average DC-Link voltage is presented in Fig. 5.12 for the considered topologies, at rated power. The NPC converter is shown as the most efficient topology with semiconductor losses counting 0.91%. The ANPC converter losses are the same as for the NPC converter when using LS-PWM or an equivalent SVM technique. An increased loss of 0.05% is when using PS-PWM, because the additional reactive power delivered to the filter inductor increases the switching losses, with a total of 0.96%.

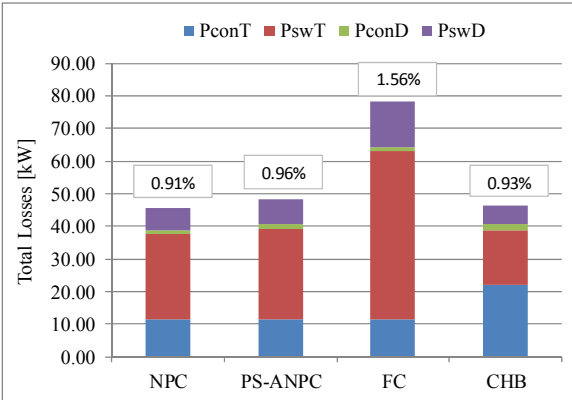


Figure 5.12.: Converters losses at average DC-link voltage

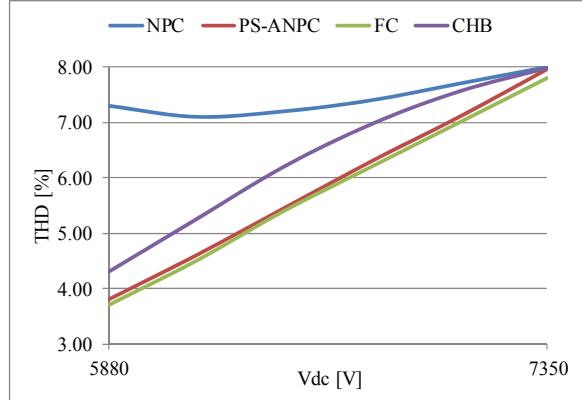


Figure 5.13.: Converters current THD for the DC-link voltage variation

The small installed switch power of the FC converter results in a substantial increase of the switching losses. Conduction losses are similar with the NPC converter, and the total FC losses are 1.56% for this particular design scenario.

The five-level CHB converter exhibits higher conduction losses due to the high number of devices in conduction per switching state. However, with a total of 0.93% semiconductor losses it is a good competitor to the three-level NPC converter. It is even more interesting considering the small required output filter. The main disadvantage is that it requires a large number of DC-link capacitors, gate drives and control signals.

To calculate the total harmonic distortion of the grid current, Eq. 5.8 was used. Here h is the harmonic order from the grid current spectrum. The current harmonic components were calculated with Eq. 5.9, where T is the analysed period and ω_0 the angular frequency of the fundamental component.

$$THD_i = \sqrt{\sum_{h=2}^n \left(\frac{i_{(h)}}{i_{(1)}} \right)^2} = \sqrt{\frac{i_{\text{RMS}}^2 - i_{(0)}^2 - i_{(1)}^2}{i_{(1)}^2}} \quad (5.8)$$

$$i_{(h)} = \frac{2}{T} \int_T i(t) \cdot e^{-j\omega_0 h t} dt \quad (5.9)$$

Converters THD for rated power over the entire DC-link voltage variation is shown in Fig. 5.13. Increased harmonics can be seen with the increase of the DC-link voltage. It must be noted that no harmonic control was applied. Using harmonic compensation in the current control loop will lead to a THD decrease due to low order harmonics reduction.

5.6. Summary

The single-stage five-level CHB, three-level NPC, ANPC and FC converters for grid connection to MV were presented in this chapter. The choice of the topologies selection, among the various possibilities that were presented in Ch. 4, was based on the number of components, capacitors voltage balancing, silicon utilization and control complexity. A comparison in terms of output voltage, semiconductors requirements, semiconductors losses and output current THD has been done for a design case scenario. The three-level NPC and five-level CHB turned out to be the most efficient topologies. Moreover, advantages for the CHB converter are the small output current THD, the minimized output filter and usage of lower voltage semiconductor devices. The NPC however, requires smaller DC-link capacitors.

The general disadvantage of the single-stage power conversion solutions is the requirement of a high voltage battery system and the necessity to overdimension in voltage rating the power semiconductors and batteries. High voltage batteries are still an unexploited researched field, which need to be addressed for the future high power battery energy storage systems. Their reliability, efficiency and feasibility are in question for the different battery technologies.

Chapter 6.

Two-Stage Cascaded H-bridge Grid Converter for Energy Storage

This chapter presents the design and control of a nine-level cascaded H-bridge converter for energy storage with bidirectional boost converters. An independent phase control is proposed and validated by simulation, structure is able to balance the capacitors voltages and the SOC of the energy storage units. Devices loss distribution in the converter cell and total loss over a wide battery voltage variation is calculated for charge/discharge operation modes

6.1. Introduction

The power grids based on decentralized power generation systems will require energy storage units, in order to balance and stabilize the power flow when a high amount of renewable energy sources are introduced. The storage units can be centralized if stationary energy storage systems are considered, or decentralized to the end users when for example the stored energy considered is in the electric vehicles batteries. Stationary energy storage systems can be installed in the vicinity of renewable sources or in critical points of the grid. This will postpone the network expansion with high voltage direct current transmission or it will reduce the transport load on the current interconnections. It will also minimize the stress on grid during peak generation hours of renewable sources [149].

For the considered system, the connection of the storage system to the grid is desired to be at medium voltage level. In this way the transmission and distribution networks can receive support from the storage system.

A system design for a battery energy storage system with 5 MW and 5 MWh as building block is considered, to be connected to the medium voltage grid via a 4.16 kV transformer. To reduce the batteries nominal discharge current it is natural to make use of series connection, fact that will also increase the batteries efficiency. However, the knowledge for series connection of batteries up to several kV is limited. At this voltage level

the cells balancing becomes a problem, and it is not a robust solution at the moment. To reduce the batteries nominal voltage, the number of series connected storage cells can be distributed in a number of converter cells making use of the Cascaded H-bridge (CHB) Converter. This will keep the possibility of medium voltage converter output, while using low voltage batteries. This advantage comes also with the drawback of the cells isolation to ground, which needs special design to reduce the capacity to ground and thus reduce the leakage ground currents.

The CHB converter was the first invented multilevel topology, patented in 1975 [100], followed up by the neutral point clamped converter in 1980 from the same inventor [107]. From its early development, the CHB converter was designed as battery charger/discharger to store energy from other generation units with higher voltages. The application to a transformerless system with grid coupling at 6.6 kV is given in [104], making use of supercapacitors in each converter cell DC-link to eliminate the disadvantage of second harmonic current drawn from the batteries.

The CHB converter disadvantage is that from its cell nature, each half bridge having the fundamental reference, the current drawn from the capacitor will incorporate a second harmonic component [150]. Furthermore, each cell capacitor will experience wide voltage variation dependent on the state of charge (SOC) for different storage technology. The batteries typical voltage variation from 5% to 95% SOC for different storage technologies is given in Table 6.1 [13].

Storage Technology	V_{max} [V]	V_n [V]	V_{min} [V]	DC-DC ratio p.u.
Li-ion / LiFePO ₄	3.60	3.30	3.20	1.13
Li-ion / LiCoO ₂	4.20	3.70	3.50	1.20
Sodium-Sulfur (NaS)	2.20	2.20	1.70	1.29
Zebra (NaNiCl)	3.00	2.58	2.25	1.30
Nickel-Metal Hydride (NiMH)	1.50	1.20	1.10	1.36
Nickel-Cadmium (NiCd)	1.50	1.20	1.10	1.36
Lead-Acid (Pb-H ₂ SO ₄)	2.50	2.00	1.75	1.48
Supercapacitors (EDLC)	2.50	2.00	1.25	2.00
Vanadium Redox Flow	1.50	1.20	0.50	3.00

Table 6.1.: Battery technologies voltage variation

It can be noticed the wide nominal voltage variation for technologies like Sodium-Sulfur, Nickel-based and Lead-Acid. Furthermore, for the electric double-layer capacitor (EDLC) and Vanadium-based Redox Flow batteries the voltage variation goes as high as 3 p.u. Wider voltage range is necessary, to cover the voltage drop on the internal impedance, in

order to charge and discharge. Therefore, the battery pack has to be over dimensioned in voltage as well as the semiconductor devices.

The CHB-based topology from Fig. 6.1 is proposed as an alternative solution which will ensure a full control on the batteries discharge current. A current controlled bidirectional boost converter is installed in each converter cell. This should operate only in continuous conduction mode to avoid the batteries microcycles.

In this way, the batteries lifetime is not affected by the ripple currents drawn by the DC-AC stage switches. Moreover, a degree of freedom is created in the battery voltage choice.

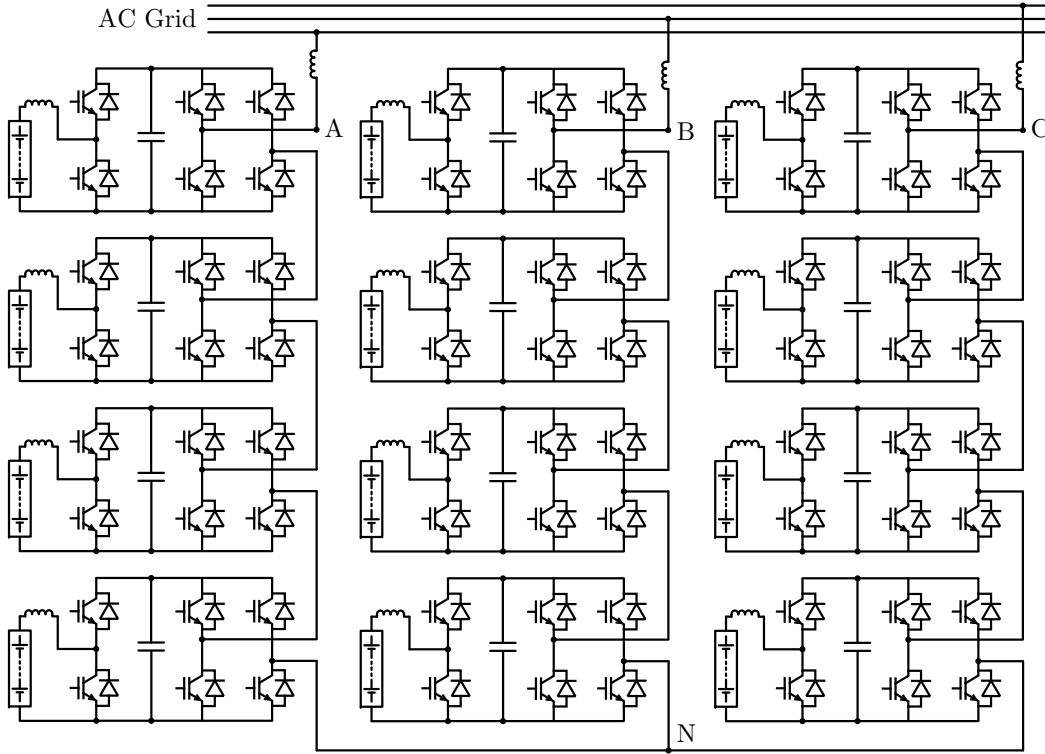


Figure 6.1.: Nine-level CHB converter with energy storage

The batteries charge/discharge current control can be additionally used to balance the DC-link capacitors in case of high cells voltage difference due to unpredicted events. However, in normal operating conditions the balance control is desired to be achieved with the DC-AC switches.

Having the cell average DC-link voltage constant, will optimize the battery size and the DC-AC stage switches. However, this improvement brings the disadvantage of reduced overall converter efficiency at full load compared with the single stage topology, due to additional losses in DC-DC converters.

6.2. Overview of CHB active rectifier control structures

For the CHB converter grid control structure, the output AC current must be synchronized with the grid voltage and the DC-link capacitors voltages must be controlled and balanced among all cells. For this purpose, different control concepts were proposed [104, 151, 152, 153].

The natural way to shift the control structures applied for two-level converters to multilevel converter is to use the control of the total DC voltage (average controller) as an outer loop to the inner control loop which controls the grid current. Thus, a proportional integrator (PI) DC voltage controller which controls the average value was employed in [104, 152]. This is normally applied to the so-called symmetrical CHB converter structures, where the cells average voltages are equal. In order to maintain the balance between different cells, balancing control of each cell is applied making use either on proportional controllers [104] or PI controllers [152]. In steady state conditions, the CHB phase-shift modulation provides a natural voltage balancing by assuring the same theoretical power output from each cell. In real conditions due to different characteristics of the used components, such as parasitic elements and different semiconductors power loss, the output/input power of different cells is slightly different. The change in voltage without balancing is very slow and therefore, the bandwidth of the balancing controllers needs to be designed as slowest from the system, not to affect the average voltage control loop and therefore the current loop.

Another control concept is to use a PI controller for the total voltage control which indirectly controls the voltage of one cell capacitors, loop which gives the grid current reference [151]. Cascade PI controllers for the other cells voltage control are used, with lower bandwidth than the total voltage controller. This control structure can be used with single phase control, with special care to be taken in the controllers design. A similar structure, making use of feed-forward terms to adjust the ratio of the different cells voltages is given in [149].

6.3. Proposed CHB control structure

The independent single phase control structure is proposed (see Fig. 6.2) for the control of the CHB-based topology from Fig. 6.1. Here the integrators for sinusoidal signals (resonant) are used for current control in natural abc frame [48, 49]. The grid voltage background distortion as well as other nonlinear effects on the current spectrum can be compensated by the current loop using current harmonic compensators.

The single phase phase-locked-loop algorithm based on second order generalized integrator is used to estimate the grid phase angle and to calculate the filtered phase voltage [35], see Sec. 2.2.2→Fig. 2.7. Since the proposed system basic function is to exchange

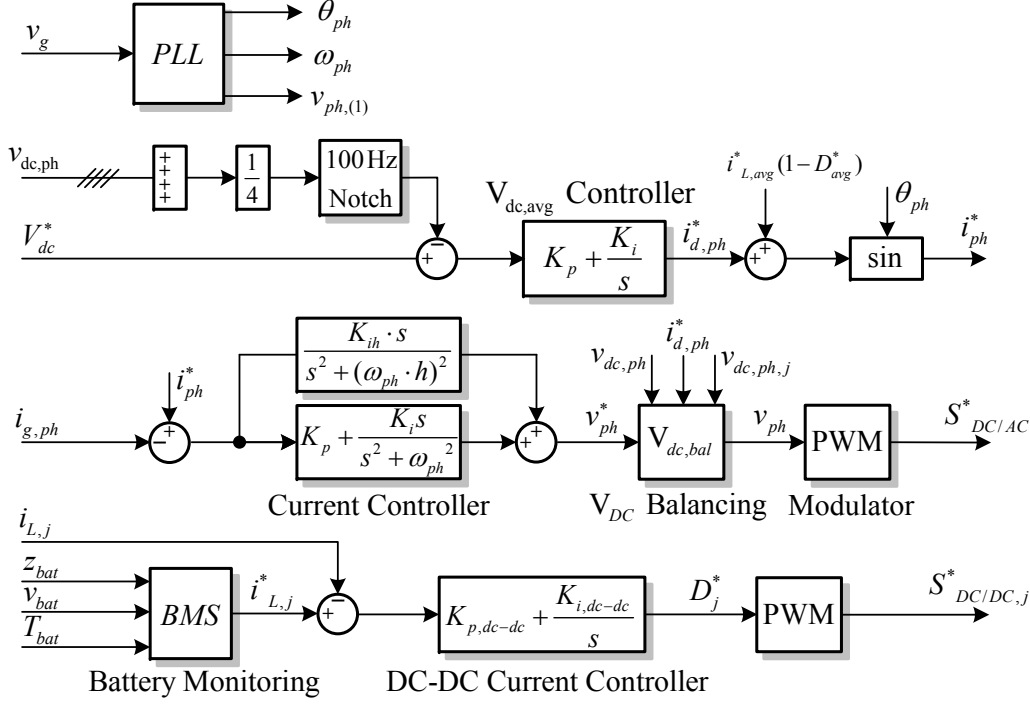


Figure 6.2.: Proposed CHB independent phase control structure

active power, the unity power factor (PF) is considered for the fundamental current component. However, the approach presented in [154] can be used to support the grid with reactive power at light or when there is no active power load. However, this will add additional stress on the converter semiconductor devices. Therefore, this additional grid service should not be provided if there is not a business case available.

Having the proposed converter topology, the second harmonic current drawn by each H-bridge is moved from the main energy storage unit to the cell DC-link. Therefore, the DC voltage control feedback needs to be filtered not to affect the current loop. This can be achieved either by averaging the voltage measurement over a half of the grid fundamental period (e.g. 10 ms), or by applying a notch filter [155], tuned at twice the fundamental frequency (e.g. 100 Hz). In first case, when averaging, the DC voltage PI controller bandwidth needs to be tuned at a frequency below the fundamental. This is usually enough for most applications and it is used in this work. Whenever faster dynamics are required, the notch filter is an alternative solution.

To improve the dynamics of the DC voltage loop, the average of the imposed DC-DC current for each phase is added in the output of the voltage controller as feed-forward term. Whenever the difference between the AC current peak value and the DC-DC current is significant, this feed-forward term should be scaled accordingly.

Since the average DC voltage controller does not assure the equal voltages of all the modules and is tuned with slow dynamics, a voltage balancing controller is employed.

The DC voltage balancing is presented in Fig. 6.3, for a converter structure with 4 cells per phase. The input average DC voltage is unfiltered in order to detect the unbalance of the cell j , which is corrected by the proportional controller $k_{p,bal}$ with the sign depending on the imposed output current. This will ensure the voltage balancing across the modules of each phase.

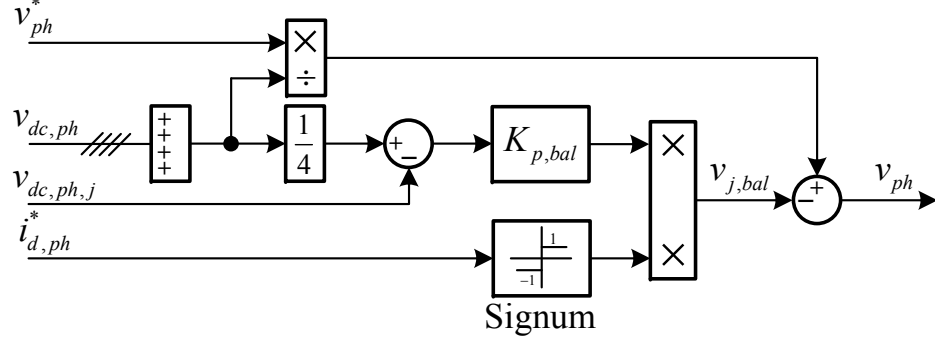


Figure 6.3.: Phase cells DC voltage balancing

The amount of unbalance is limited by the converter DC voltage reserve. Therefore, in a special case of large deviation in the output power of different cells, either the total DC voltage reference needs to be increased or the battery current reference can be adjusted accordingly to support the maintenance of the balance operation.

As modulation strategy, the phase shifted modulation gives a straight forward implementation [104] and is adopted in the following. For optimization of switching losses the selective harmonic elimination can be applied [152].

The battery current reference is decided by the battery monitoring system (BMS) which limits the reference current depending on current battery state of charge. The control of the bidirectional boost converter of each cell is achieved with an average PI current controller, see Fig. 6.2. When the DC-DC converter current reference is reduced and therefore when the converter active power transfer is reduced or stopped there is the possibility to deliver ancillary services.

6.4. Converter model

In Table 6.2 the circuit parameters are shown for the considered nine-level CHB converter topology, comprising of 4 converter cells per phase with one bidirectional boost converter in each. The grid coupling is transformerless to the 4.16 kV line, while a standard boost AC transformer will be used to connect to a 10/20 kV. The grid filtering requirement in case an L filter will be used is only 0.5 mH (4.5%). The maximum current total harmonic distortion (THD_i) is 2.9% at rated power and linear load.

Rated active power	P	5 MW
AC grid line voltage	V_{LL}	4.16 kV
Rated rms current	I	694 A
Rated AC frequency	f	50 Hz
Grid filter inductance	L_f	0.5 mH (4.5%)
Cell capacitance	C	10 mF
Cell inductor	l_b	3 mH
Battery rated voltage	V_b	480 V
Battery maximum current	i_b	1050 A
Number of cells per phase	n	4

Table 6.2.: Circuit parameters of the nine-level CHB converter with energy storage

A battery is installed in each cell and has a nominal voltage of 480 V and a voltage variation between 400 V and 550 V depending on the SOC. The boost inductor is rated at 3 mH, having the switching frequency 2100 Hz, double compared with the DC-AC switches, for a 5% maximum charge/discharge ripple current over the entire voltage variation.

6.5. Simulation results

A simulation model with the circuit parameters from Table 6.2 was built in PLECS [22] to validate the proposed control method and to compute the semiconductor devices losses. Table 6.3 shows the control parameters used in simulation. The H-bridge is switched with 1050 Hz and a deadtime of 5 μ s with the measurements sampled twice per each switching period (regular double edge sampling).

6.5.1. Performance of the proposed control strategy

The operation when 5 MW flows to the grid, at unity power factor and nominal battery voltage ($V_{bat} = 480$ V), is shown in Fig. 6.4. The phase quantities of the grid voltage are shown in Fig. 6.4.(a), while the converter's phase to neutral voltages are shown in Fig. 6.4.(b). It can be seen the effect of the second harmonic current on the capacitors voltages from Fig. 6.4.(d). The cells voltages are in groups of 4 balanced voltages for each phase with the ripple phase shifted with 120 degrees, having a total of 12 traces. The shape of the converter voltages are also due to the capacitors voltage variation, and

Average voltage control proportional gain	$K_{p,DC}$	2 A/V
Average voltage control integral time	$T_{i,DC}$	40 A/V·s
Voltage feedback averaging time	$T_{avg,DC}$	10 ms
Voltage balancing proportional gain	$K_{p,bal}$	0.02
Current control proportional gain	$K_{p,i}$	1.5 V/A
Current control resonant gain	$K_{res,i}$	1000
Proportional gain for DC-DC current control	$K_{p,DC-DC}$	0.01 V/A
Integral gain for DC-DC current control	$K_{i,DC-DC}$	1 V/A·s
Switching frequency for H-bridges	$f_{sw,AC}$	1050 Hz
Switching frequency for DC-DC bridges	$f_{sw,DC-DC}$	2100 Hz
Sampling time	T_S	1/(2·1050) s

Table 6.3.: Control parameters of the nine-level CHB converter with energy storage

this has a small negative impact on the grid current THD_i when compared with the ideal operation from Fig. 6.7.

The minimum converter cell DC-link voltage for inverting mode operation and maximum for rectifying mode, is given by Eq. 6.1, where n is the number of converter cells.

$$V_{DC,avg,min_{inv}} = V_{DC,avg,max_{rect}} = \frac{\sqrt{2}}{2n} V_{LL} = 735 \text{ V} \quad (6.1)$$

To transfer the rated power of 5 MW to the grid, the nominal cell DC-link voltage is 775 V which covers all the voltage drops and keeps a 5% modulation index as reserve.

In this operation mode the DC-DC converters references are the same, assuming the SOC over the cells as balanced. Fig. 6.4.(e) shows 12 traces of the batteries discharge currents. The grid condition under this simulation is ideal and therefore the harmonic content of the grid current is mainly due to the pulse-width-modulation and deadtime with the compensation of 5th and 7th harmonics. The grid current THD_i in this operation mode is 2.9%.

The charging behaviour is shown in Fig. 6.5, operating at negative unity power factor. Identical negative current references are given to the DC-DC converters. Similar to the previous case, it can be seen the capacitors and output voltage ripples dependent on the load current and shifted with 180 degrees at this time. The grid current THD_i is 2.67% in this operation mode.

In the first two case scenarios, the SOC of different cells was assumed to be identical. To prove the control operation to correct the converter cells SOC unbalance, different SOC

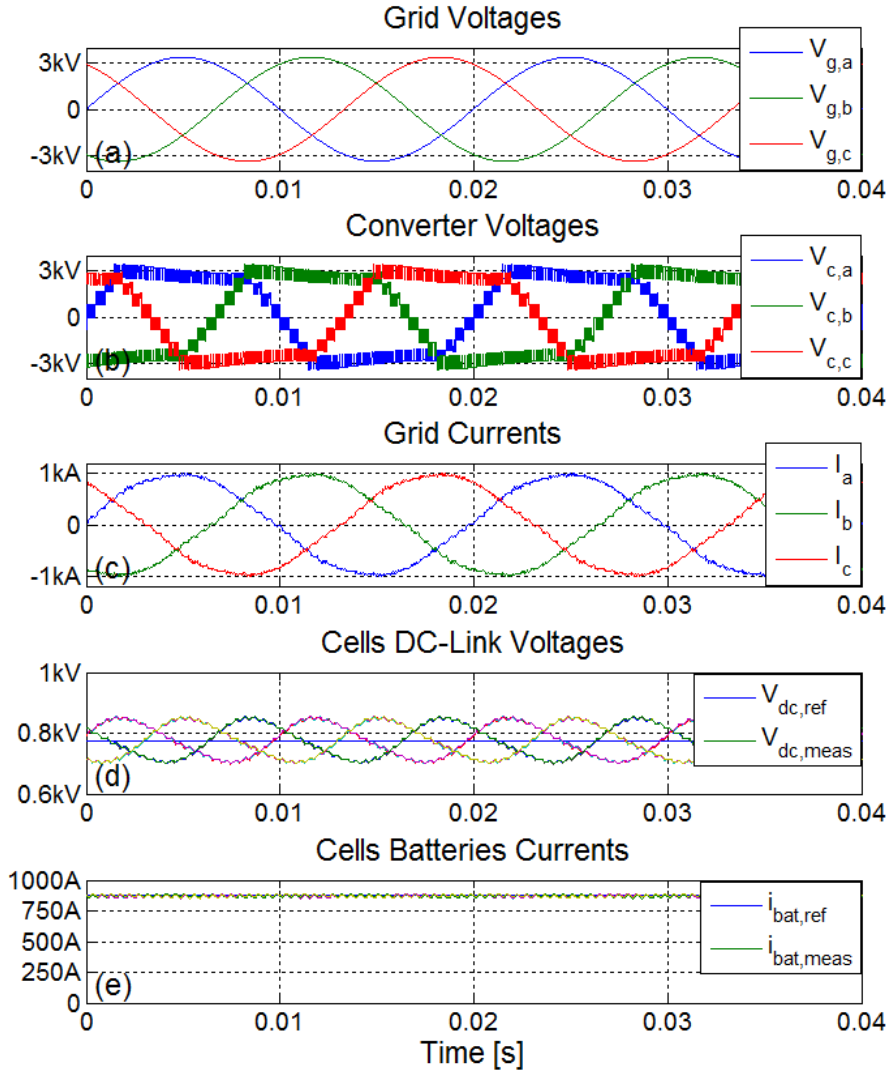


Figure 6.4.: Nine-level CHB converter operation during discharge

over the cells of phase a are considered. In Fig. 6.6 it is shown the converter operation to correct the SOC differences. To maintain the same output AC power, the cells with higher SOC are discharged with higher currents compared with the average DC-DC reference current and respectively the cells with lower SOC are discharged with lower currents. The cells discharge currents are shown in Fig. 6.6.(c). For cell 1 the current reference with respect to the average is lower with 20 A, for cell 2 is lower with 40 A for cell 3 is higher with 20 A and for cell 4 higher with 40 A. Thus symmetrical operation against unbalance is implemented. Fig. 6.6.(d) shows the phase a DC-link voltages. It can be noticed that the DC-link voltages are balanced within a narrow tolerance band, while all keeping the 100 Hz ripple which cannot be mitigated. Therefore, the output power contribution of different cells is different and this can be seen also in the modulation indexes of the phase a cells from Fig. 6.6(e).

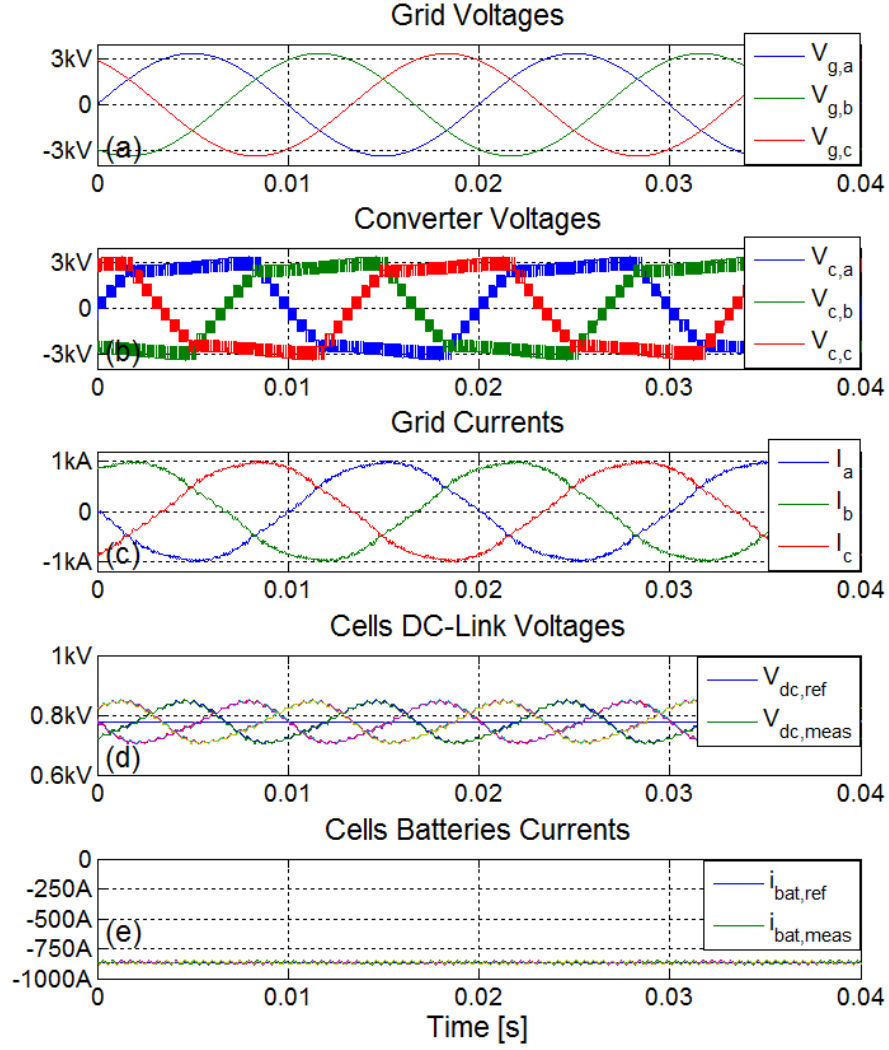


Figure 6.5.: Nine-level CHB converter operation during charge

The amount of unbalance is limited by the converter voltage reserve. Therefore, the control must ensure balanced SOC at all times and should reduce the average voltage reference as much as possible to reduce switching losses. For different output powers, different average voltage references should be given.

Considering the installation of a 1 F supercapacitor in each converter's cell DC-link to take over the 100 Hz pulsed power, the converter operation during discharge is shown in Fig. 6.7. This is an ideal operation with reduced DC-link voltage ripple and therefore reduced output converter voltages ripple. This leads to a reduction of the grid current THD_i down to 0.8%. Thus, with more than 2% smaller THD_i compared with the operation mode from Fig. 6.4. The harmonic compensation for the low frequencies is still necessary in order to reduce the deadtime effect on the grid current.

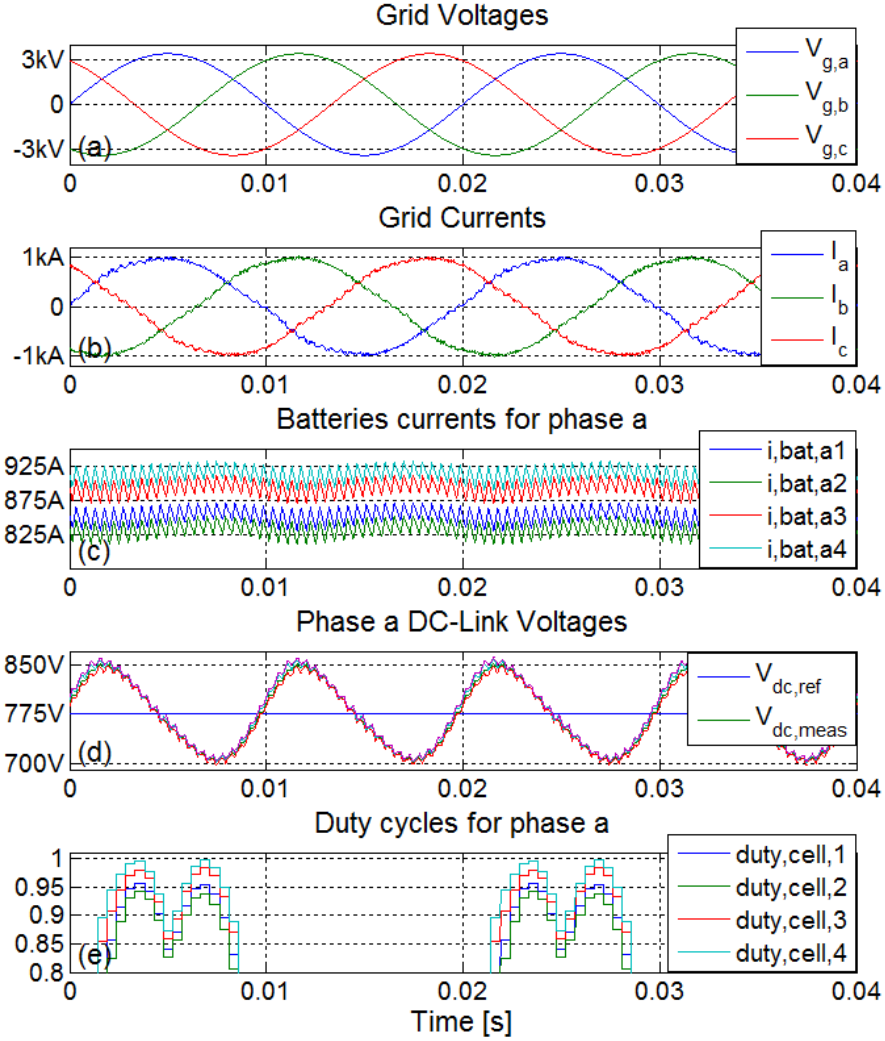


Figure 6.6.: Nine-level CHB converter SOC and DC voltages balancing

6.5.2. Power semiconductor loss analysis

The semiconductor losses were calculated for the steady state operation under balanced batteries SOC, at rated power. The cell devices notation is shown in Fig. 6.9. The considered cell IGBT modules are the fourth generation 1700 V, 1200 A (FZ1200R17HP4) from Infineon. The maximum junction temperature is $T_j = 150^\circ\text{C}$ with the junction to case thermal model given in the Foster network, having four thermal impedance points given in the datasheet [146]. The implemented thermal chain is shown in Fig. 6.8, where the thermal resistances and time constants are taken from the datasheet. Considering an adaptive cooling system, the heat sink temperature is assumed to be constant at $T_h = 80^\circ\text{C}$.

Semiconductor loss distribution for a converter cell at nominal battery voltage and unity

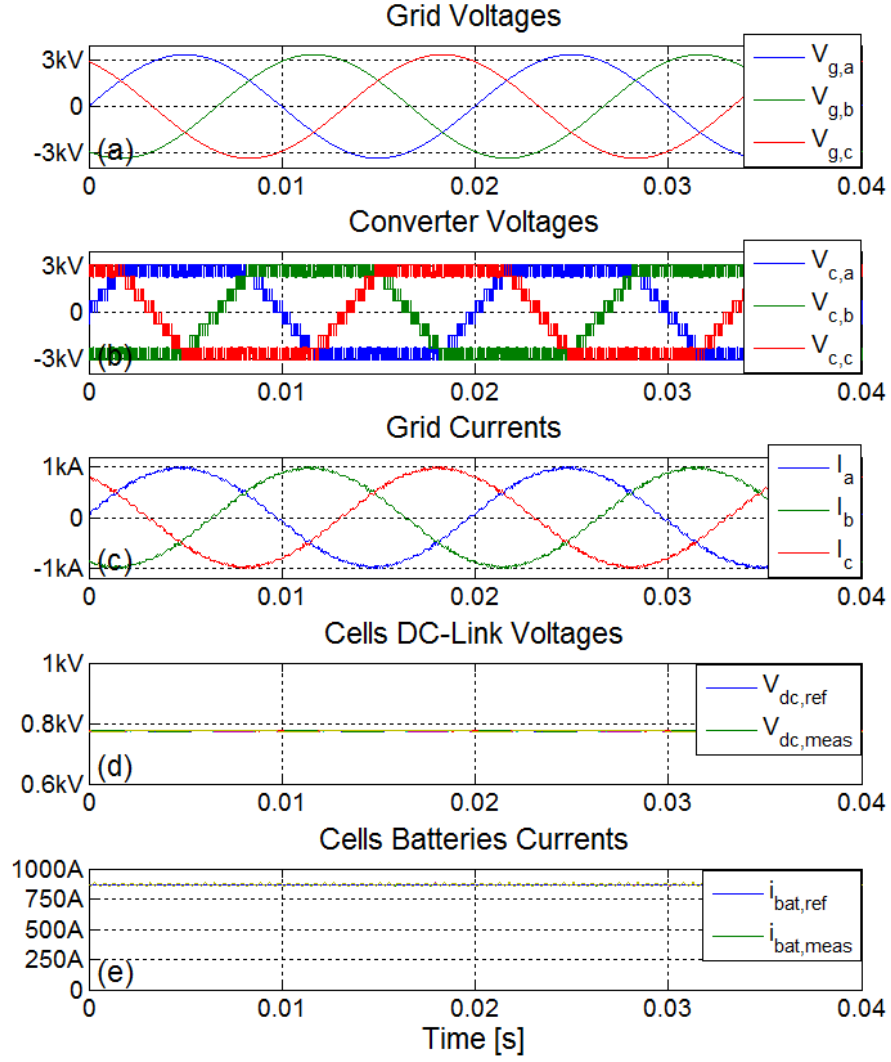


Figure 6.7.: Nine-level CHB converter operation with 1F DC-link supercapacitor

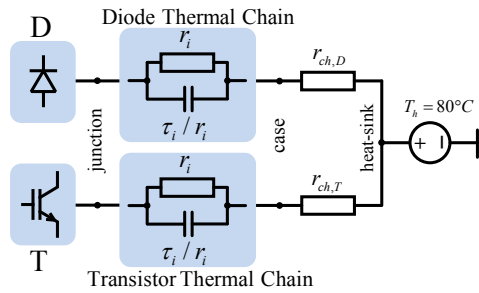


Figure 6.8.: IGBT module thermal circuit

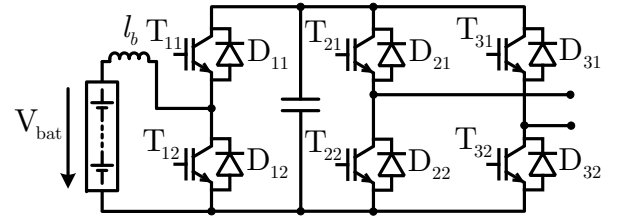
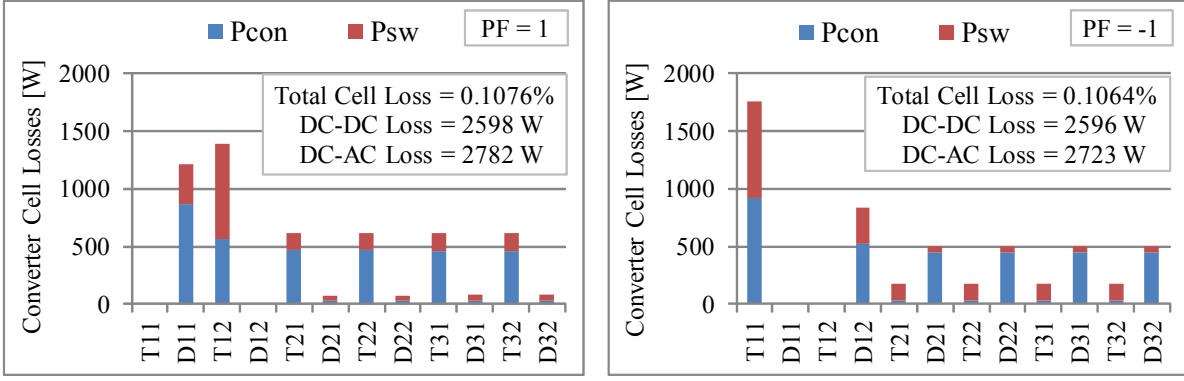


Figure 6.9.: Converter cell

power factor is shown in Fig. 6.10, for inverting and rectifying modes.

In the inverting mode ($\text{PF} = 1 \rightarrow \text{discharge}$), the DC-DC converter is in the boost mode

Figure 6.10.: Converter cell loss distribution at $V_{bat} = 480$ V

and therefore only diode D_{11} and transistor T_{12} experience losses. The H-bridge losses are mainly in transistors, where the high number of series connected devices (8 per switching state) results an increase in conduction losses. However, the H-bridge switching losses are small (see Fig. 6.10). It can be noticed the increased losses of the DC-DC converter devices, which is around double compared with the H-bridge switches for the used switching frequency and boost ratio. Therefore, an improved implementation will require two interleaved DC-DC converter legs that can share the losses.

The loss distribution in case of rectifying operation ($PF = -1 \rightarrow$ charge) is also shown in Fig. 6.10. The buck transistor T_{11} is the most loaded device. In the H-bridge devices the conduction losses are distributed to diodes.

In Fig. 6.11 the semiconductor losses are shown, over the entire battery voltage variation, for inverting and rectifying operation modes.

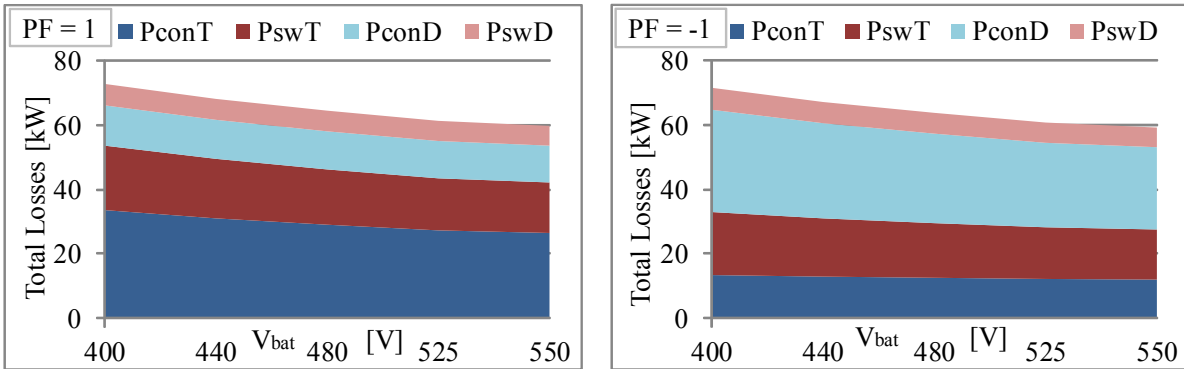


Figure 6.11.: Total converter losses for charging and discharging operation modes

The charge/discharge considered mode is with constant power, therefore the battery current will vary from 760 A at the highest voltage up to 1051 A at the lowest voltage. Thus, the semiconductors efficiency varies from 98.54% discharging and 98.57% charging

at lowest battery voltage, up to 98.8% discharging and 98.82% charging at the highest battery voltage.

It is noticed an efficiency decrease compared with a single-stage CHB conversion system described in Ch. 5. However, the battery nominal voltage can be reduced to low levels where the maturity and reliability are well proved in industry. When a low DC-link capacity is installed, the battery current ripple is kept in a region where the lifetime is not affected. Furthermore, when looking at the entire system losses, the power electronic is a highly efficient system compared with the battery system. The battery efficiency for instance is as low as 60% for Nickel-based technologies and Redox-Flow, and it can go as high as 95% for Lithium-ion battery.

6.6. Summary

The cascaded H-bridge converter with an integrated energy storage unit controlled by a bidirectional boost converter was investigated. The independent phase control composed of single phase DC voltage control, synchronization and current control was proposed and validated by simulation. The converter topology and its control structure allows the balance of converter cells capacitors voltages and the state of charge of the energy storage units.

With a 4.5% installed output L filter, the grid current THD_i was below 3% with the H-bridge transistors switched at 1050 Hz. The operation with supercapacitors installed in each cell DC-link has shown the best performance, reducing the cells ripple voltage and the grid current THD_i .

The cell semiconductor loss distribution was calculated at nominal energy storage unit voltage and the total converter loss was calculated over the entire battery voltage variation. It is noticed a slight decrease in efficiency for the proposed two-stage topology (98.54%–98.82%) compared with a single stage CHB conversion system (99.07%). However, the battery nominal voltage can be reduced to low levels where the maturity and reliability are well proved in industry. Furthermore, when a low DC-link capacity is installed, the battery current ripple is kept in a region where the lifetime is not affected. When looking at the system level the losses in the power electronics are very small compared with the losses in the energy storage technologies.

Chapter 7.

New Modular Multilevel Converter with Integrated Energy Storage

This chapter introduces a new modular converter with integrated energy storage based on the cascaded half-bridge modular multilevel converter with common DC bus. Converter grid control structures will be applied, to validate the possible power flows. The inter-connection of a DC and AC grid with bidirectional power flow, where both of them can receive or generate excess power to the energy storage units integrated in each converter sub-module will be demonstrated in this chapter with particularities for each operating scenario

7.1. Introduction

One of the most important hybrid converter concept introduced in the last years is the combination of the cascaded H-bridge and flying capacitor converters, in the cascaded half-bridge (ChB) with common DC-bus converter (also called Modular Multilevel Converter (M2C)) [128, 156]. Due to its modular construction based on half-bridge cells, this topology is optimal for medium and high voltage [156].

Considering a centralized storage system, based on battery building blocks, with a power rating in the range of MW and energy in the range of MWh which is connected to medium voltage the converter solutions can be classified into:

- High voltage battery with NPC/ANPC converter [15]
- Low voltage modular batteries with series connected dual active bridges [96] and NPC/ANPC converter [157]
- Low voltage modular batteries with CHB converter [104]

Having a controlled ambient temperature, batteries voltage variation depends mainly on their state of charge (SOC). The typical variations from 5% to 95% SOC for different batteries technologies were given in Ch. 6→Table 6.1. Thus, for the direct conversion

with NPC centralized converter or modular CHB converter, the battery nominal voltage and the converters nominal DC-link voltage needs to be oversized to enable the required grid power transfer. In the solution with modular batteries and dual active bridges, only the DC side is modular but not the grid interface which is a centralized NPC/ANPC converter. This is a disadvantage which imposes restrictions in the system scalability on both storage units and converter.

This chapter introduces a complete modular concept to interface low or medium voltage batteries to the medium or high voltage grids. This enables a flexible scaling of converter modules with integrated energy storage and power electronics to a wide range of operating voltages, output power and stored energy. Having the modular construction with controllable sub-module, the converter topology is not dependent on the used storage technology. The converter control structures are applied in this chapter, to validate the possible power flows.

7.2. New Modular Multilevel Converter Concept

To achieve a complete modular converter structure with building blocks constructed from batteries and power electronics, the cascaded half-bridge topology [128] was considered as a host for this purpose. With the highest degree of modularity, the converter structure from Fig. 7.1 is moving the centralized stored energy from the conventional main DC-link to distributed smaller voltage rating DC-links [128, 156]. This fact allows in the converter design to eliminate the leakage inductance locally for the used semiconductors. However, this improvement comes up with price paid in increased total installed capacitors. The inherent circulating current between phases required to charge the cells capacitors with the lowest voltages and discharge the cells capacitors with the highest voltages.

Figures 7.2, 7.3, and 7.4 show three of the possible converter cell structures, as power electronics and energy storage building blocks. The basic converter cell from Fig. 7.2, is the solution with the reduced number of active components. The half-bridge switches (S_1 and S_2) with the DC-link capacitor from the host configuration are in charge to transfer the power in or out from the converter cell. The second half bridge switches (S_3 and S_4) form a bidirectional boost converter with its inductor, as additional components to charge or discharge the energy storage unit integrated in the cell. Depending on the energy storage unit characteristic, and the chosen control bandwidths, this can be used to control the voltage of the cell capacitor C . If the pulsating currents has a negative effect on the storage unit lifetime, the bridge must be current controlled at a constant level. In this case, the capacitor will be in charge to absorb the in-out pulsating energy.

An extended solution is shown in Fig. 7.3, where the interleaved bidirectional boost converter will reduce the inductor current ripple and thus its core size. As it was seen in Ch. 6→Fig. 6.10, the cell loss distribution when using a single DC-DC converter bridge is uneven. Sharing the operating current the losses are distributed to the two legs

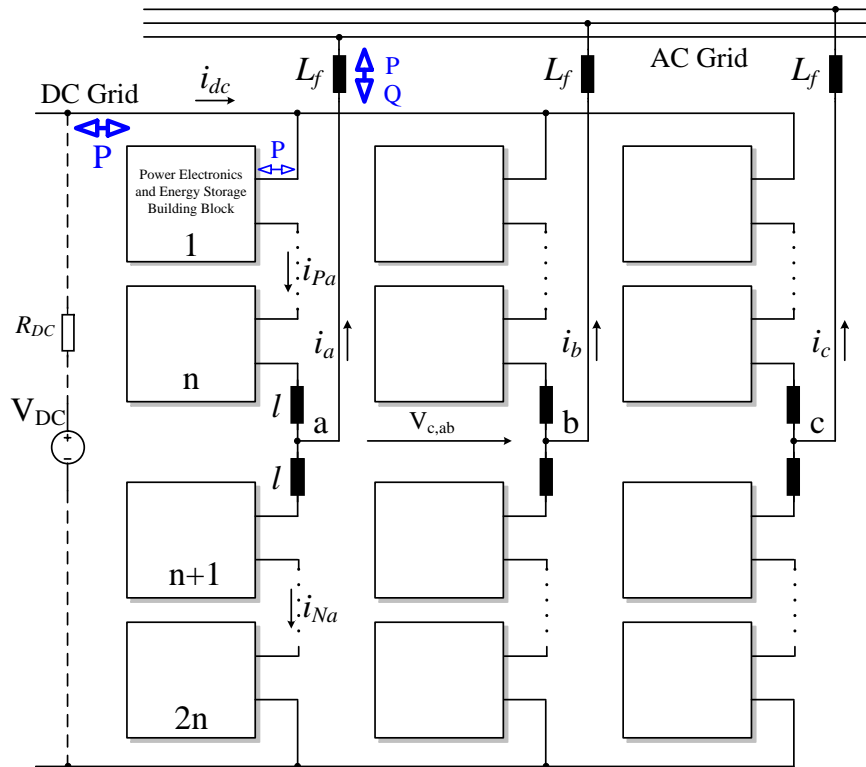


Figure 7.1.: New Modular Multilevel Converter with Integrated Energy Storage

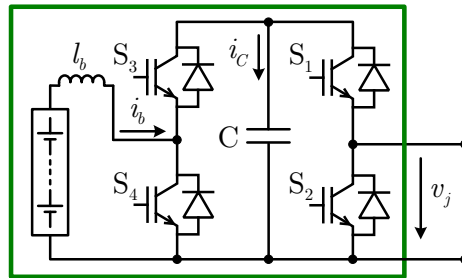


Figure 7.2.: Converter cell with reduced component count

and this is suitable for increased transfer power with the storage unit. However, the overall efficiency is not optimal due to the high switching losses in the DC-DC converter devices.

Based on the dual active bridge (DAB) converter [96], the optimized converter cell for high efficiency and high boost ratios is shown in Fig. 7.4. The half-bridge on the higher voltage side of the DC-DC converter is a voltage doubler and must be designed with higher voltage and smaller current rated devices while the full bridge on the low voltage side designed with lower voltage and higher current rating.

When the cell nominal DC-link voltage goes up to higher levels there is the necessity to

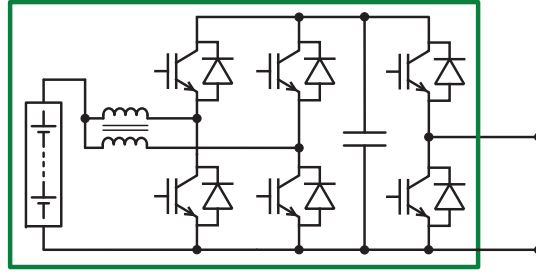


Figure 7.3.: Interleaved boost DC-DC converter cell

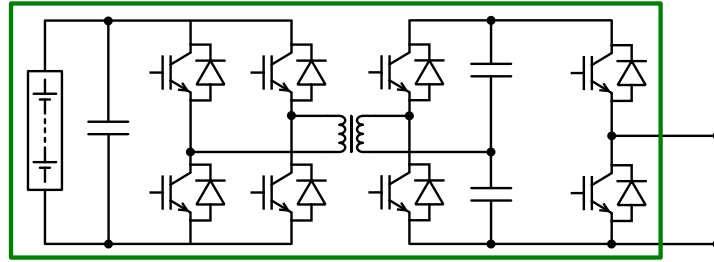


Figure 7.4.: Voltage doubler DAB based converter cell

realize a serial connection of the half-bridge devices. To avoid the active balancing of the series connected devices, the DC-DC converter approach presented in Ch. 3→Fig. 3.1 can be used.

With the disadvantage of overall increased number of components, the advantages of the solution presented in Fig. 7.4 are obvious, such as:

- Usage of significant lower voltage energy storage units compared with the total DC-AC output voltages
- Reduced switching losses due to soft-switching, within the operating boundary
- Galvanic insulation with medium or high frequency transformer reduces safety concerns and reduces the batteries leakage currents due to ground coupling capacitances

Having the described cells, it is possible to transfer power between any of the three main power sources namely: the higher voltage DC (e.g. DC grid or wind turbine DC-link), the AC grid and the distributed energy storage units from the converter cells. The basic converter cell from Fig. 7.2 is considered in the followings, for reduced number of active devices and control simplicity.

7.3. Converter Operation and Control Methods

The converter with the circuit from Fig. 7.1 will always verify the following equation, applied for any of the a , b or c phase legs:

$$V_{DC} = \sum_{j=1}^{2n} v_j + l \frac{d}{dt} (i_P + i_N) \quad (7.1)$$

Here, V_{DC} is the main DC bus voltage, v_j is the cell output voltage, $2n$ is the number of cells per phase leg, l is the arm inductance, i_P and i_N are the positive (cells $[1]..[n]$) and respectively negative (cells $[n+1]..[2n]$) arms currents. Considering the cell from Fig. 7.2, when the switch S_1 is turned ON and S_2 is OFF the cell is said to be inserted and the cell output voltage is equal with the capacitor voltage. In complementary when S_2 is turned ON and S_1 turned OFF the cell is bypassed and the output voltage is nearly zero, equal with the conducting device ON state voltage drop. The converter switching states must always ensure that the number of inserted cells must be equal with the number of bypassed cells and equal with n . The output AC current i_{AC} , is equal with the sum of the arm currents (7.2), while a circulating current i_Z between DC buses or between phases is given in (7.3).

$$i_{AC} = i_P - i_N \quad (7.2)$$

$$i_Z = \frac{1}{2} (i_P + i_N) \quad (7.3)$$

The circulating current, charges the cells with the lowest voltages and discharges the cells with the highest voltages. Therefore, one method to balance the capacitors voltages is to control this current [129]. On the basis of equations (7.2), (7.3) the capacitive energy storage balance between the upper and lower arms can be achieved by controlling independently the voltage contributions on each [130].

7.3.1. Modulation Strategies

Space Vector Modulation

The universal concept of the space vector representation of converter output voltage levels can be applied for any multilevel converter with theoretical expansion to any number of levels. The complexity increases with high number of levels, where number of the redundant vectors increases [158]. The state transition can be controlled to reduce the line voltage ripple, and therefore the current ripple. For the present converter it is possible to implement a switching state sorting algorithm for capacitors voltage balancing [131]. The decisions are taken by choosing cells with the extreme deviation from their nominal set point depending on the current direction, to charge or discharge them [128]. The result is an $n + 1$ level in the phase voltage and $2n - 1$ in the line.

Level Shift Pulse Width Modulation

For converter configurations with n number of cells per arm, there are necessary $n - 1$ carrier signals where half are level shifted up and half down with respect to zero which are compared with reference signal [159]. The result is an $n + 1$ level phase output voltage. The disadvantage is that the conduction times are normally uneven distributed per cells. Therefore the capacitors voltage balancing can be achieved rotating cells from one carrier to another and can only be applied successfully at high switching frequencies.

Phase Shift Pulse Width Modulation

For converter configurations with n number of cells per arm, one possibility is to use $2n$ carrier signals with $360^\circ/2n$ phase shift. The reference for the positive arm is negative and the reference for the negative arm is positive when the power flow is from the DC to AC, similar to the unipolar modulation. In this way the number of voltage levels in the phase voltage is $2n + 1$ and $4n + 1$ in the line voltage, with the first switching harmonics centred at $2n \cdot f_{SW}$, where f_{SW} is the chosen switching frequency. Two proportional integral (PI) controllers are required for each phase to control the average voltage through the circulating current, while a proportional controller for each cell balancing must be used [129]. This results in a difficult implementation, and brings limitations in the chosen switching and sampling frequencies. An alternative solution is presented in Fig. 7.5, and used in this chapter.

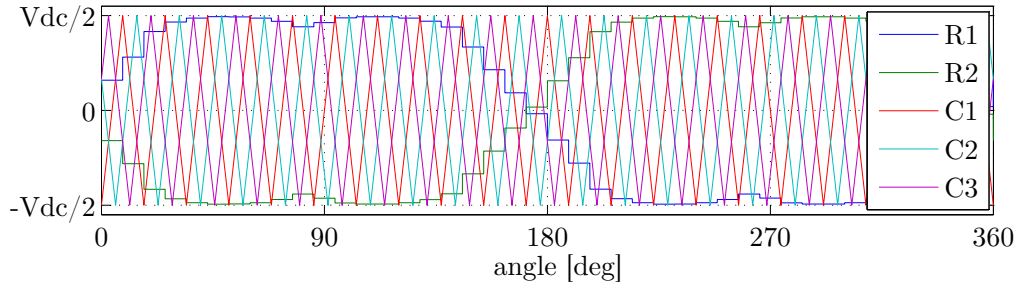


Figure 7.5.: References and carrier signals for a phase shift PWM alternative

The reference signals are used as previously with the particularity that $n/2$ carriers with $(360^\circ/n) \cdot 2$ phase shift are used for both the positive and negative arms duty cycles generation. Grouping cells from positive and negative arms to the same carrier leads the achievement of even duty cycle distribution and therefore a simpler voltage balancing is required over the fundamental frequency similar to the flying capacitor converter [121]. This advantage comes up with the drawback of reduced number of levels to $n + 1$ for phase and $2n + 1$ for the line voltages, with the first switching harmonics at $2 \cdot f_{SW}$.

Selective Harmonic Elimination Pulse Width Modulation

Selective harmonic elimination PWM (SHE-PWM) has been a research subject for half a century, after introduction in 1960's [160], and generalized in [161]. When applied to a two-level converter, the only concern is to eliminate certain harmonics from the output voltage spectrum. However, when used for a cascaded half [162] or H-bridge [152] converter the DC-link capacitors voltage balancing is the a supplementary concern that must be addressed. It was shown that this modulation strategy can be applied also for the cascaded half-bridge converter, with an average switching frequency of 150 Hz [162]. A voltage balancing mechanism similar to the SVM technique can be implemented to select a redundant voltage state, which maintains the equilibrium between the input/output power of all converter cells. However, this can only be applied when the number of cells is high enough to provide the sufficient redundancy. It was shown that for a converter with $n = 10$ cells (11-levels) is possible to cancel the low order harmonics and maintain the DC voltage balance [162].

7.3.2. Current Control

The AC current control dynamics is described by (7.4) for any of the a , b or c phases, where the R_{ech} and L_{ech} are the equivalent resistance and inductances for the output filter and grid, V_g is the grid voltage and V_c the converter phase produced, imposed for instance by the reference given in (7.5).

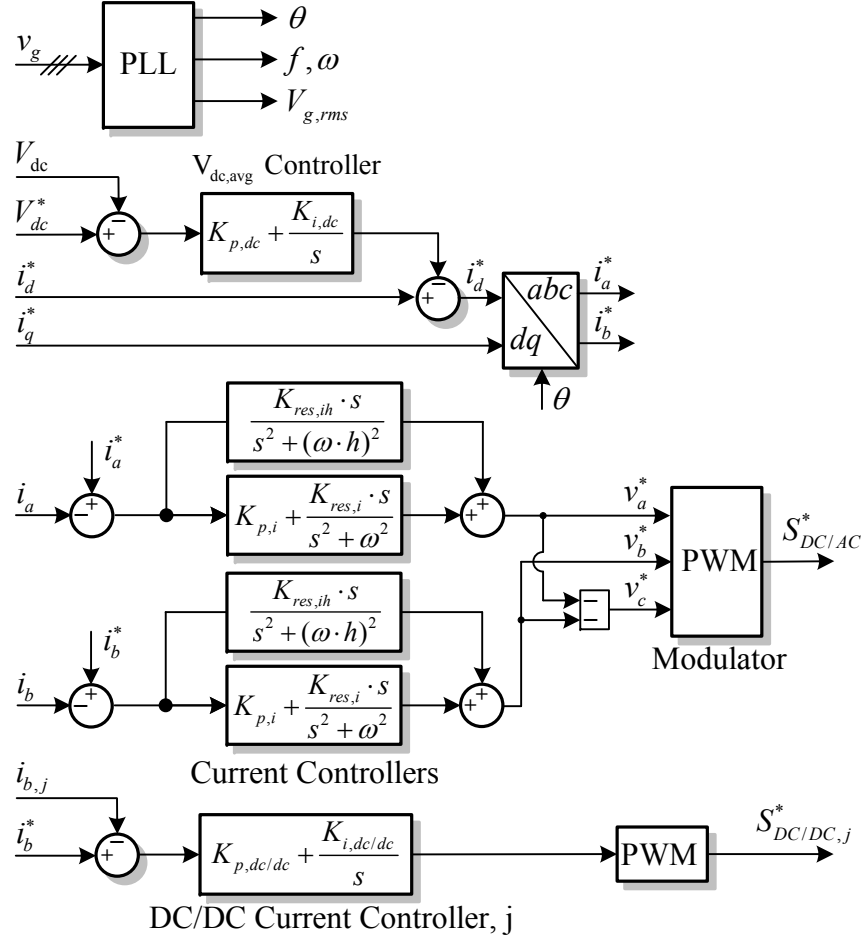
$$\frac{d}{dt}i_g(t) = -\frac{R_{ech}}{L_{ech}}i_g(t) + \frac{1}{L_{ech}}(V_c(t) - V_g(t)) \quad (7.4)$$

$$V_{c,ref} = \frac{V_{dc}}{2} + m\frac{V_{dc}}{2}[\sin(\omega t + \phi) - \frac{1}{2} \cdot (\max[V_{c,ref,abc}] + \min[V_{c,ref,abc}])] \quad (7.5)$$

Having this, with the modulation strategy that makes sure the cells voltages are balanced, theoretically any of the current control strategies can be used with particular features and dynamics [163]. The abc current control structure is used here [49], which makes use of proportional resonant controllers, see Fig. 7.6. The control is performed on two of the three phase currents while the third one is indirectly deduced. When the grid unbalanced condition is a concern, a third controller can be employed.

7.3.3. DC Voltage Control

A PI controller is employed to control the average voltage regulation at a decoupled smaller bandwidth than the inner current control loop. The current references are calculated using the dq/abc transformation with the rotation angle given by a phase-locked-loop algorithm. Depending on the required transfer power, the DC voltage reference must


 Figure 7.6.: Applied *abc* frame grid converter control structure

be adapted to keep the energy stored in the converter to a minimum, fact that will enhance the efficiency for various operating points. The control of the DC power flow when connected to a DC grid controlled by other means the reference is given by Eq. 7.6 [5]:

$$V_{dc}^* = V_{DC} + R_{DC} \cdot i_{DC} \quad (7.6)$$

7.3.4. DC-DC Converters Control

Switches S_3 and S_4 are used to control the energy storage charging/discharging current. When the transistor of S_3 with the diode of S_4 conducts current alternately, the current i_b is negative. In complementary when the transistor of S_4 with the diode of S_3 conducts current alternately, i_b is positive. Since the energy storage units may be sensitive to low frequency ripple currents, depending on the used technology, the voltage mode control

is not considered in this work. Therefore, an average PI current controller regulates the charge/discharge current for each cell, as shown in Fig. 7.6.

7.4. Operation Modes and Their Performance

Three operation modes can be defined with this converter structure, depending on the power flow and the control requisite of the involved power sources:

- a) DC grid to/from AC only - inverting control structures for ChB [128, 156]. The DC source is controlled by other means and the intervention of the energy storage unit is on request;
- b) Energy storage units to/from AC only - the high voltage DC source is not present, this representing a pure energy storage converter mode;
- c) Bidirectional power transfer between any of: DC grid, energy storage and the AC grid.

To analyse the converter behaviour under the defined operation modes, the parameters from Table 7.1 are considered in the simulated converter model. Thus, 600 V energy storage units are connected to medium voltage DC and the AC grids.

In the *operation mode (a)* the corresponding transistors S_3 and S_4 of all cells are turned OFF normally, and the exchange power is between the DC and AC grids. In Fig. 7.7 this operation mode is illustrated, for unity power factor and nominal transferred power, where the power flow is from the DC grid to the AC grid. This is the state of the art power transfer case, described in [128, 156, 129, 131, 159], which is applied for the basic configuration of the ChB converter.

In the performed simulation from Fig. 7.7 it is considered that the DC voltage is supplied to the converter terminals, and is controlled by other means. Therefore, the DC controller is disabled and the AC current control with the parameters given in Table 7.2 calculates the voltage references for the required power transfer.

In Fig. 7.7.(a) are shown the AC grid line voltages and the converter line voltages are presented in Fig. 7.7.(b). It can be noticed the converter behaviour as voltage source, when the buffer inductor is kept as small as necessary to reduce the peak circulating current (100 μ H in this case) and therefore optimized for the operating frequency at twice the output alternating frequency. To reduce the core size of the buffer inductor, if any, the coupling of the upper and lower inductor for each arm can be done. However, with a low inductance value, the output currents must receive smoothening from an output filter, L filter in this case.

In Fig. 7.7.(c) the AC grid currents are shown, and in Fig. 7.7.(d) the phase a current quantities are shown for the positive and negative arms (i_{Pa} , i_{Na}) and the sum of them as phase a grid current (i_a). It can be noticed the dominant fundamental frequency

Rated active power	P	5 MW
AC grid line voltage	V_{LL}	4.16 kV
Rated RMS current	I	694 A
Rated AC frequency	f	50 Hz
DC grid voltage	V_{dc}	6 kV
DC grid resistance	R_{dc}	1 Ω
Arm inductance	l	100 μ H
Grid filter inductance	L_f	1.3 mH
Cell capacitance	C	4 mF
Cell inductor	l_b	6 mH
Storage unit rated voltage	V_b	600 V
Storage unit rated current	i_b	240 A
Cell capacitor rated voltage	V_c	1 kV
Number of arm cells	n	6

Table 7.1.: Model parameters of the ChB with integrated energy storage

Voltage control proportional gain	$K_{p,DC}$	0.5 A/V
Voltage control integral time	$K_{i,DC}$	100 (A/V·s)
Current control proportional gain	$K_{p,i}$	1.5 V/A
Current control resonant gain	$K_{res,i}$	1000
DC-DC current control proportional gain	$K_{p,DC-DC}$	0.01 V/A
DC-DC current control integral time	$K_{i,DC-DC}$	1 (V/A·s)
Switching frequency for AC devices	$f_{sw,AC}$	1050 Hz
Switching frequency for DC-DC devices	$f_{sw,DC-DC}$	2100 Hz
Sampling time	T_S	1/(2·1050) s

Table 7.2.: Control parameters for the ChB with integrated energy storage

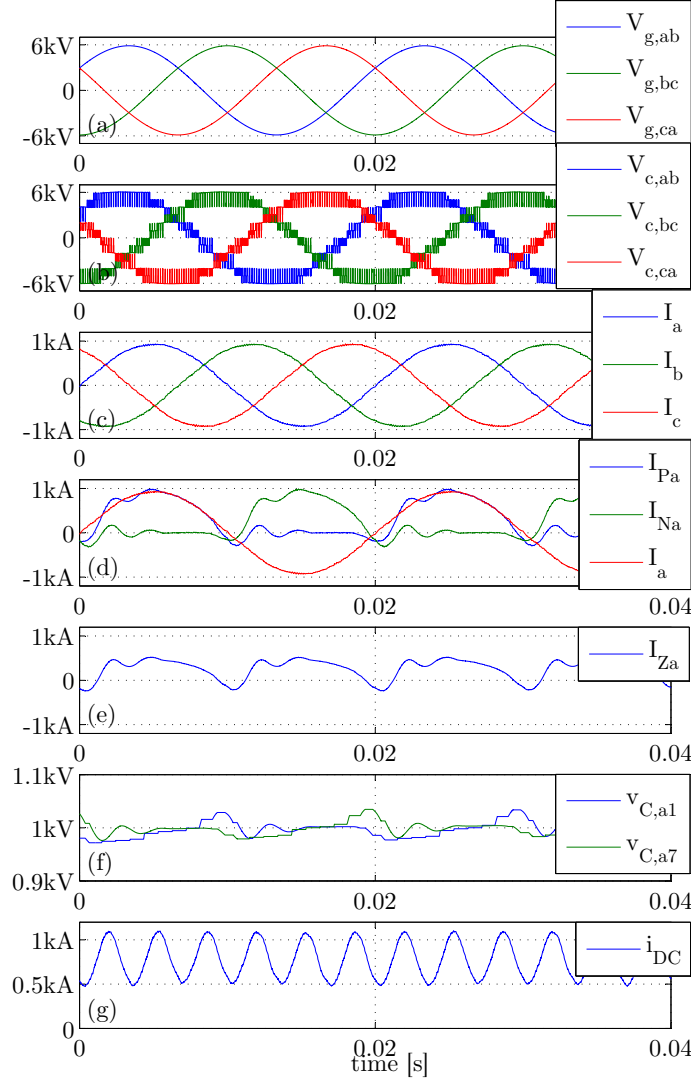


Figure 7.7.: Mode (a): Power transfer between AC and DC grids

components of the arm currents on their conduction period, with a very low share of second and fourth harmonics. Fig. 7.7.(e) shows the phase a circulating current (i_{Za}), which basically shapes the voltage ripple of the capacitors from Fig. 7.7.(f). The DC grid current (i_{DC}) from Fig. 7.7.(g) shows an alternating frequency of 300 Hz (6th harmonic) with a positive DC offset, when considering the annotation from Fig. 7.1. This is an important disadvantage of this topology, a high installed DC capacity will be required to reduce the DC grid voltage ripple. However, considering a HVDC application, the DC-link cable is a capacitor itself which reduces this concerns to a certain level.

Operation mode (b) is illustrated in Fig. 7.8, where the power transfer is between the energy storage units and the AC grid. This resembles the converter functionality as an energy storage system for the AC grid. Here the DC voltage controller is enabled and

regulates the voltage to maintain the power balance between the interconnected sources. The currents of the storage units are controlled to a constant level with the same control parameters to all cells, as given in Table 7.2.

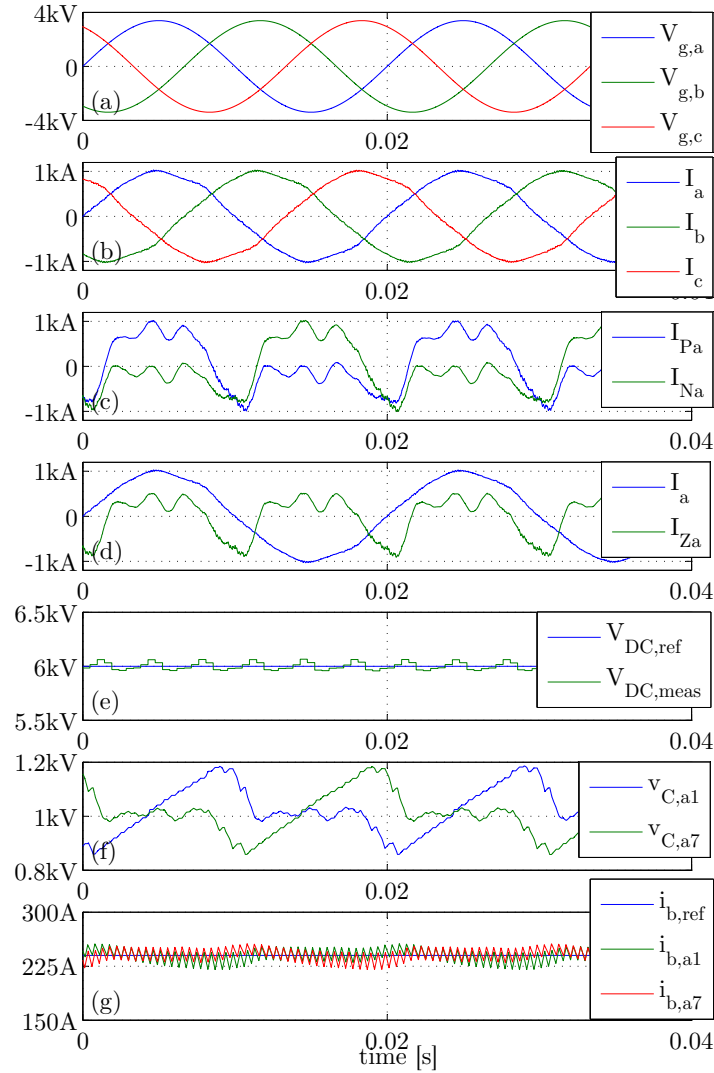


Figure 7.8.: Mode (b): Power transfer between energy storage units and AC grid

Fig. 7.8.(a) shows the AC grid phase voltages and Fig. 7.8.(b) the grid currents. In Fig. 7.8.(c) the positive and negative arms currents are shown. It can be noticed in this operation mode, with the selected buffer inductance, that the arms currents present an increase of the second harmonic. The RMS values of the 1st and 2nd harmonics are comparable, while multiples of second harmonic are also present in the spectrum at lower levels. This can also be deduced looking at the circulating current from Fig. 7.8.(d), which is reflected by the capacitors voltage ripple shown in Fig. 7.8.(f) ($v_{C,a1}$ and $v_{C,a7}$ from the positive and respectively the negative arms). The cells capacitors energy storage oscillation will take over the excess/lack of power, which is translated in an increase of

the voltage ripple. The over dimension in the installed capacity is not desired. Therefore, at this level of the voltage ripple, a capacitor technology which can accept this oscillation must be used in the converter design - e.g. film capacitor technology.

Operation mode (c) is shown in Fig. 7.9, where the power transfer between all power sources (converter cells - energy storage units, the DC grid and the AC grid) is shown. Here, half the rated power (2.5 MW) is transferred from the energy storage units to both the DC and AC grids.

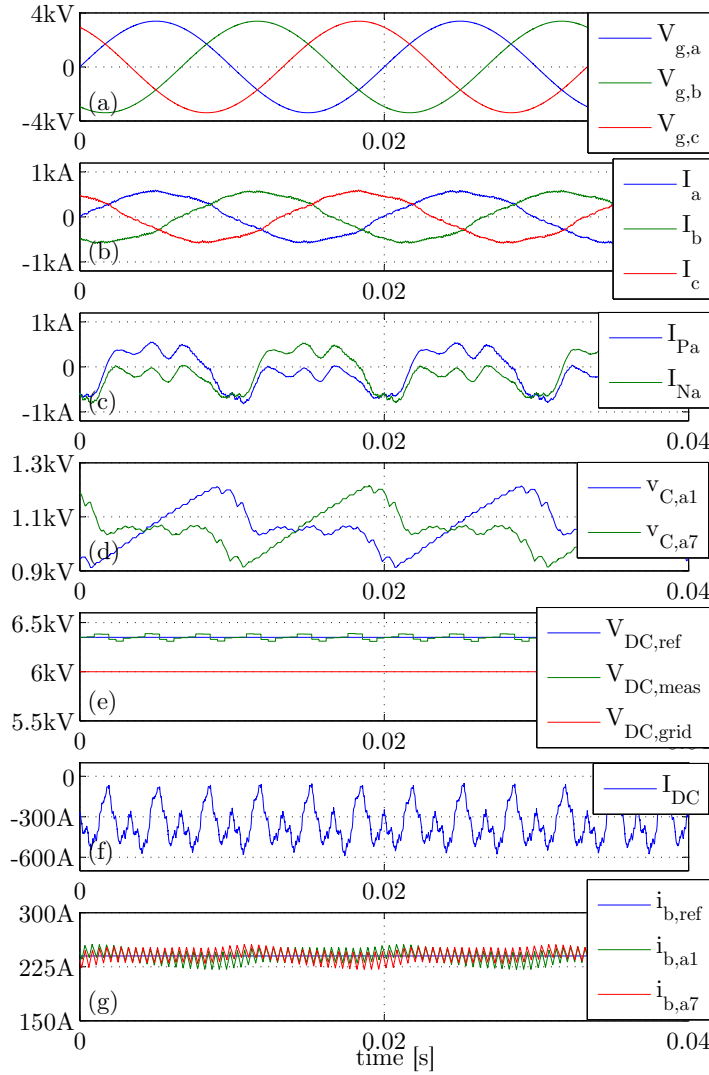


Figure 7.9.: Mode (c): Power transfer between energy storage units, DC and AC grids

The DC voltage is controlled according to Eq. 7.6 and both the DC and AC grids receive 2.5 MW each, half the converter rated power. This particularity enables the converter usage as a high voltage UPS system in the future high voltage direct current (HVDC) meshed grids, for both the AC and DC grids where it is connected.

In Fig. 7.9.(a) and Fig. 7.9.(b) are shown the phase quantities of the AC grid voltages and respectively the AC grid currents. In Fig. 7.9.(c) the phase *a* arm currents are shown. Here the second harmonic in the is dominant over the fundamental frequency. The fundamental frequency is reduced, proportional to the AC grid current RMS value, which is in this case controlled to a half from the rated power.

The capacitors voltage ripple is similar to *operation mode (b)*, shown in Fig. 7.9.(d) for two cells of the phase *a*. The control of the DC-link voltage according to Eq. 7.6, for a power transfer of 2.5 MW to the DC grid, is shown in Fig. 7.9.(e). The injected DC grid current is shown in Fig. 7.9.(f). Because of the increased 2nd harmonic current in the arms currents, makes the DC grid current to have not only the 6th harmonic over the DC offset as in *operation mode (a)*, but also the 12th harmonic. The current control for two of the bidirectional boost converters from phase *a* is shown in Fig. 7.9.(g). A small impact of the capacitors voltage ripple is observed in the measured currents, however with far below the specified 5% ripple normally given for instance in the batteries datasheets [13].

7.5. Energy Storage System Construction Concept

Fig. 7.10 shows a modular energy storage system construction concept, with converter cells integrating the power electronic devices, energy storage and processing units. The control of the DC-DC converters are processed locally in each cell with a lower quality processing unit (Slave #). The overall control and set-points are computed with the high quality processing unit (Master). All units are connected to a communication bus from where the duty cycles and charge/discharge current references are updated from the master control platform and the feedback is sent back with information like: fault report, capacitor voltage level, state of charge, state of health. This gives the possibility to construct a complete modular system.

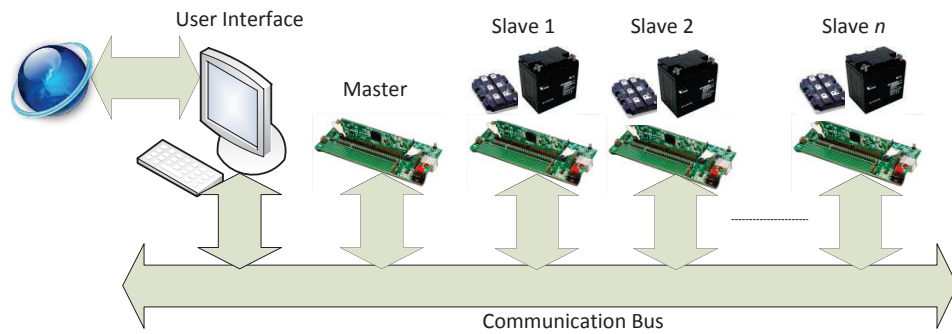


Figure 7.10.: Modular energy storage system construction concept

One possibility to implement the communication bus is the Controller Area Network (CAN), which is a standard communication protocol in commercial DSP systems [164,

165]. It was shown that is feasible to be used, and the implementation for a 6.6 kV, 1.4 MW, 13-level CHB converter is given [166].

7.6. Storage System Design Considerations

Considering a battery energy storage system, the parasitic elements must be considered in the design phase. Fig. 7.11 shows the parasitic capacitances to ground (C_p) for batteries, and their potential difference to ground. When the distance d between battery housing and battery shelf is null, the capacitance is the highest, the impedance to ground is the lowest and therefore leakage ground currents i_{leak} will be at the highest levels. The potential difference between battery terminals and ground, is with respect to the common mode voltage $V_{cell,cmv}$ of each cell, and is particular for each cell position within the converter.

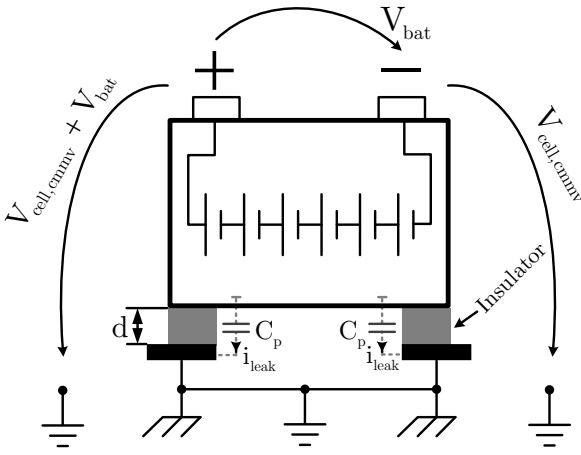


Figure 7.11.: Battery parasitic capacitances to ground

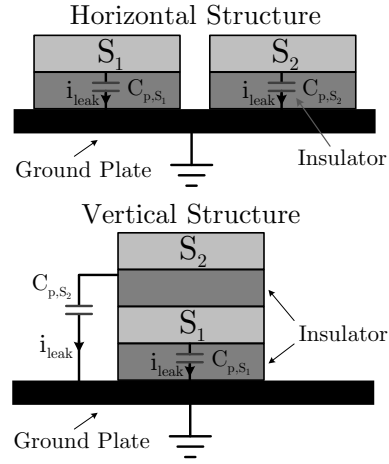


Figure 7.12.: Semiconductor parasitic capacitances to ground

In Fig. 7.12 the semiconductor parasitic capacitances to ground are shown, for the horizontal and vertical structures [167]. In the horizontal structure, the parasitic capacitances are similar ($C_{p,S1} \cong C_{p,S2}$). The device with the highest potential to ground will experience the highest leakage current but also will change the collector potential faster, when IGBT switches are considered. For the vertical structure, $C_{p,S1} > C_{p,S2}$ and therefore the leakage current for the device S_2 will be smaller.

Fig. 7.13 shows typical converter cells common mode voltage to ground for phase a . It can be noticed the wide differences between cells, depending on the position in the converter arms.

These parasitic elements are critical for the system reliability, efficiency and the EMI performance. At each switching state transition, the converter cell potential to ground

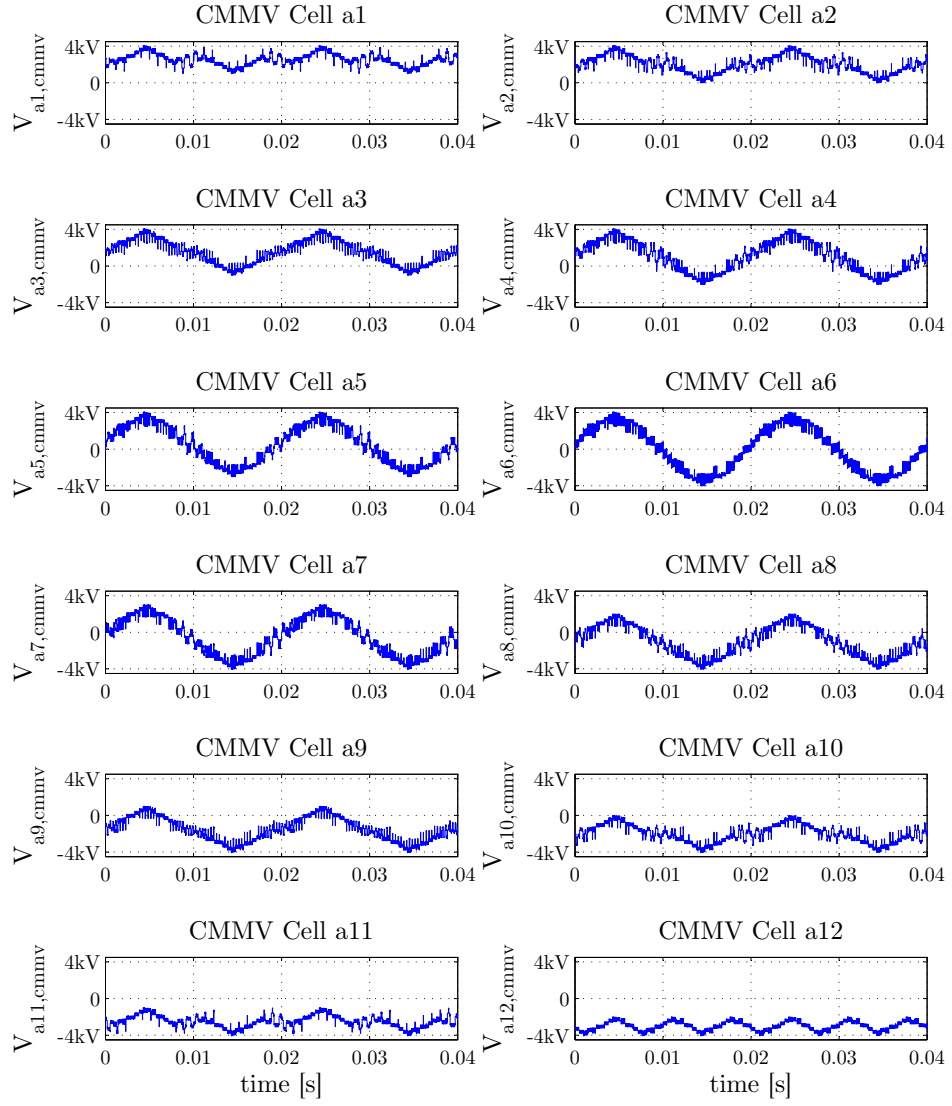


Figure 7.13.: Cells common mode voltage to ground for phase a

changes. Therefore, leakage currents will flow to ground, currents proportional with the applied dV/dt . Measures to reduce the parasitic capacitances have to be used. As an example, for batteries, an insulation material placed between batteries and shelf will significantly reduce the capacitance.

7.7. Summary

A new modular multilevel converter structure with integrated energy storage was introduced in this chapter. This converter structure is suitable to interface low and medium

voltage energy storage units to medium and high voltage grids. This represents a complete modular solution with energy storage and power electronics building blocks. Furthermore, the topology is independent on the energy storage characteristic, since each cell can be independently controlled. Therefore, the scaling in voltage, power and energy levels have many degrees of freedom.

The converter functionality and control structures was presented. Three operation modes were identified and implemented in a simulation model. The interconnection of a DC and AC grid with bidirectional power flow, where both of them can receive or generate excess power to the energy storage units integrated in each converter sub-module was demonstrated.

A new modular energy storage system construction concept was introduced. This enables the complete modularity implementation of the proposed converter topology, with power electronics, energy storage and distributed processing units. Furthermore, the challenges on the storage system design were addressed to enable an efficient and reliable converter operation.

Part III.

Conclusions

Chapter 8.

Conclusions and Future Work

8.1. Summary and Conclusions

This work was divided in two parts, CONTROL OF DC-AC GRID CONVERTERS and MEDIUM VOLTAGE GRID CONVERTERS FOR ENERGY STORAGE. The first part starts with a brief review of control strategies applied to grid connected DC-AC converters. A control implementation was realized for a 100 kW active rectifier. In the second part, different solutions for power converters to interface energy storage units to medium voltage grid are given. A new modular multilevel converter was introduced, where the energy storage units are integrated in each converter cell.

A survey on the main control principles for grid connected converters was given in Ch. 2. Firstly the general control structure with its main building blocks is shown. Single-phase and three-phase PLL methods were reviewed. Three-phase PLL methods are widely used in three-phase converter due to a simplified implementation and reduced computational burden. Single-phase PLL methods can be used in special cases for three-phase converters when the processing power is available and if the topology requires the independent phase control.

Linear and nonlinear current control methods were presented. Linear control methods are widely used in the industry, such as the rotating dq frame. The generation of reference signals is very important, and must be carefully implemented. Nonlinear methods emerge in the control of grid converters, due to a optimized control with respect to a given criteria. The required application, control complexity and the available computation power are limitations that define the usage of a specific control method.

The second harmonic ripple on the DC-link must be taken into consideration when designing the DC voltage control loop. Moreover, with the trend to reduce the installed capacity and therefore reduce the decoupling between the supply and load, the proper DC voltage control must be ensured.

The design, control and experiment of a LV DC-AC grid converter was presented in Ch. 3. The implementation was realized for a 6 kV battery energy storage test bench,

with a rated power of 100 kW. The DC-AC grid converter is in charge of controlling the common DC-link voltage and the grid currents. The grid connection was realized via an equivalent LCL filter and the stationary frame $\alpha\beta$ current control was implemented. The system was proved to be stable without damping. Increased harmonic distortion of the grid current, at light load, was seen around the frequency where the current control bandwidth is tuned. However, at rated power operation it is expected that the system will be more damped and these harmonics will be reduced below the limits of the grid connection harmonic standard. The complete test bench functionality with bidirectional power flow of up to 100 kW was also verified and presented.

A survey on hard-switched and soft-switched multilevel converters was given in Ch. 4. Multilevel voltage source converters can be found in different configurations. In principle, the building cells for multilevel converters are: two-level half bridge, two-level H-bridge, neutral point clamped and flying capacitor derived from two-level converter using series connected switches with clamping elements. Combining these building blocks, new hybrid converter concepts can be designed. Modular converters can enhance the availability, at the cost of a high amount of capacitors, gate drives and semiconductor devices required for construction.

The single-stage five-level CHB, three-level NPC, ANPC and FC converters for grid connection to MV were presented in Ch. 5. The choice of the topologies selection was based on the number of components, capacitors voltage balancing, silicon utilization and control complexity. A comparison in terms of output voltage, semiconductors requirements, semiconductors losses and output current THD has been done for a design case scenario. The three-level NPC and five-level CHB turned out to be the most efficient topologies. Moreover, advantages for the CHB converter are the small output THD, smaller output filter and usage of lower voltage semiconductor devices. The NPC however, requires smaller DC-link capacitors.

The general disadvantage of the single-stage power conversion solutions is the requirement of a high voltage battery system and the necessity to overdimension the voltage rating of the power semiconductors and batteries. High voltage batteries are still a not well researched field. Their reliability, efficiency and feasibility are in question for different battery technologies.

To avoid the aforementioned challenges, two stage modular converter topologies were proposed in Ch. 6 and Ch. 7. Based on the CHB converter, a nine-level topology with energy storage units in each converter cell was investigated in Ch. 6. The independent phase control composed of single phase DC voltage control, synchronization and current control was proposed and validated by simulation. The converter topology and its control structure allow the balance of converter cells capacitors voltages and the SOC of the energy storage units. The cell semiconductor loss distribution was calculated at nominal energy storage unit voltage and the total converter loss was calculated over the entire battery voltage variation. It is noticed a slight decrease in efficiency for the proposed two-stage topology (98.54%–98.82%) compared with a single stage CHB conversion system

(99.07%). However, the nominal battery voltage can be reduced to low levels where the maturity and reliability are well proved in industry. Furthermore, when a low DC-link capacity is installed, the battery current ripple is kept in a region where the battery lifetime is not affected.

When looking at the system level the losses in the power electronics are rather small compared with the losses in the energy storage technologies.

A new modular multilevel converter structure with integrated energy storage was introduced in Ch. 7. This converter structure is suitable to interface low and medium voltage energy storage units to medium and high voltage grids. This represents a complete modular solution with energy storage and power electronics building blocks. Furthermore, the topology presents low dependency on the energy storage characteristic, since each cell can be independently controlled. Therefore, the scaling in voltage, power and energy levels have many degrees of freedom.

The converter functionality and control structures were presented. Three operation modes were identified and implemented in a simulation model. The interconnection of a DC and AC grid with bidirectional power flow, where both of them can receive or generate excess power to the energy storage units integrated in each converter sub-module was demonstrated.

A new modular energy storage system construction concept was introduced. This enables the complete modularity implementation of the proposed converter topology, with power electronics, energy storage and distributed processing units. Furthermore, the challenges on the storage system design were addressed to enable an efficient and reliable converter operation.

8.2. Future Work

Control of grid converters with nonlinear techniques such as predictive or passivity based control is emerging. Advantages such as the reduction of operating switching frequency, improved dynamics when necessary, as well as robustness against grid impedance variation, are important. Their application to multilevel converters was limited so far and this could be an interesting topic for future research.

Multilevel converters are used in industry more and more, in an increasing variety of applications. Development of these converters advances together with the advancement in power electronic devices. However, in high power applications there are still challenges that need to be addressed as future research: control with very low switching frequency, devices voltage stress, loss distribution and thermal management, device fault detection and reconfiguration as well as fault handling.

The proposed two-stage modular converter topologies are not experimentally investigated in the literature yet. Therefore, a multilevel converter test bench using a reconfigurable converter cell should be used to investigate these topologies further.

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A1. Space Vector Transformations

1. Clarke Transformation

Direct Clarke Transformation

Natural abc frame \rightarrow Stationary $\alpha\beta$ frame:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (1)$$

Inverse Clarke Transformation

Stationary $\alpha\beta$ frame \rightarrow Natural abc frame:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \quad (2)$$

2. Park Transformation

Direct Park Transformation

Natural abc frame \rightarrow Rotating/Synchronous dq frame:

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (3)$$

Stationary $\alpha\beta$ frame \rightarrow Rotating/Synchronous dq frame:

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \quad (4)$$

Inverse Park Transformation

Rotating/Synchronous dq frame \rightarrow Natural abc frame:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) \\ \cos(\theta + \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} v_d \\ v_q \end{bmatrix} \quad (5)$$

Rotating/Synchronous dq frame \rightarrow Stationary $\alpha\beta$ frame:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} v_d \\ v_q \end{bmatrix} \quad (6)$$

3. Unbalanced signals decomposition

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = V^+ \begin{bmatrix} \cos(\theta) \\ \cos(\theta - \frac{2\pi}{3}) \\ \cos(\theta + \frac{2\pi}{3}) \end{bmatrix} + V^- \begin{bmatrix} \cos(\theta) \\ \cos(\theta + \frac{2\pi}{3}) \\ \cos(\theta - \frac{2\pi}{3}) \end{bmatrix} + V^0 \begin{bmatrix} \cos(\theta) \\ \cos(\theta) \\ \cos(\theta) \end{bmatrix} \quad (7)$$

$$v_{\alpha\beta} = v_{\alpha\beta}^+ + v_{\alpha\beta}^- = e^{j\theta} \cdot v_{dq}^+ + e^{-j\theta} \cdot v_{dq}^- \quad (8)$$

A2. Instantaneous Powers Calculation

Active and reactive powers, from the pq theory, for balanced three-phase system:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \frac{3}{2} \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{3}{2} \begin{bmatrix} v_d & v_q \\ -v_q & v_d \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{3}{2} \begin{bmatrix} v_a & \frac{1}{\sqrt{3}}(v_b - v_c) \\ v_b & \frac{1}{\sqrt{3}}(v_c - v_a) \\ v_c & \frac{1}{\sqrt{3}}(v_a - v_b) \end{bmatrix}^T \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (9)$$

Active and reactive powers, from the pq theory, for unbalanced three-phase system:

$$p = \frac{3}{2} \cdot (v_d^+ \cdot i_d^+ + v_q^+ \cdot i_q^+ + v_d^- \cdot i_d^- + v_q^- \cdot i_q^-) \quad (10)$$

$$q = \frac{3}{2} \cdot (v_q^+ \cdot i_d^+ - v_d^+ \cdot i_q^+ - v_q^- \cdot i_d^- + v_d^- \cdot i_q^-) \quad (11)$$